

CONTROL DATA® 6600 COMPUTER SYSTEM DATA CHANNEL EQUIPMENT

~~6602-B/6612-A~~, 6603-B, 6622-A,
6681-B, 6682-A/6683-A,
S.O. 60022, 60028, 60029

DIAGRAMS &
CIRCUIT DESCRIPTION

Address comments concerning this
manual to:

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or use Comment Sheet in back of this
manual.

[illegible]

FOREWORD

Logic diagrams contained in this manual do not attempt to show the entire device, nor even depict complete modules within that device. The purpose of the diagrams is to show the logical significance of circuits that may involve parts of many modules on several chassis. Logic hardware that is not pertinent to the particular logic

sequence being illustrated is not included. Certain areas may not be shown at all, while others may appear on several drawings. These limitations are important to remember; the logic diagrams do not replace the 6000 Series chassis and cable tabs, but they are a valuable tool in understanding the tabs and the overall operation of the machine.

GENERAL CONTENTS

	Key to Logic Symbols
6602/6612	Console Display Controller
6603	Disk System Controller
6622	Magnetic Tape Transport Controller (626)
6681	Data Channel Converter (3000 Series Interface)
6682/6683	Satellite Coupler
S. O. 60022	6000 Series Data Channel Converter (1612 Printer)
S. O. 60022	6000 Series Data Channel Converter (170 Card Punch)
S. O. 60028	6000 Series 1 x 4 607 Tape Transport Controller
S. O. 60029	6000 Series 405 Card Reader Controller

S. O. = Special Option

KEY TO LOGIC SYMBOLS

(Standard 6000 Series Card Types)

Logic diagrams represent a symbolic approach to electronic schematics. By using symbols to represent building block circuits, the schematic becomes easy to read if the reader understands the function of the symbols. In CONTROL DATA* logic, two signals, a logical "0" and a logical "1" are the possible input or output conditions of a circuit. For example, "1" is considered "up" and "0" is considered "down" on a timing chart. Detailed descriptions of logic symbols and their associated electronic representations are contained in the Printed Circuit Manual, Cordwood Modules (Pub. No. 60042700).

STANDARD LOGIC SYMBOLS

Standard logic diagram symbols for Control Data equipment using 6000 Series card types are inverters, test points, flip-flops, twisted pair line drivers, and coaxial cable line drivers.

Inverters

An inverter is a logic element which provides an output that is a negation of its input. When more than one input is provided to an inverter, "0's" take precedence over "1's" and therefore drive the output of the inverter to "1". Because all of the several inputs have to be "1" to drive the output of the inverter to a "0", the inverter may be considered an inverting AND (or NAND) gate when more than one input is present. The basic inverter is shown in the logic diagrams as an arrow into either a circle or a square (Figure 1). Both symbols represent the same electronic circuit and have the same logic interpretation. In a logic sequence of inverters, circle and square symbols are usually alternated as an aid in tracing signals, e.g., a "1" output from a square symbol implies a "1" output from subsequent squares in the logic chain.



Figure 1. Inverter Symbols

Certain card types employ variations of the standard inverter building block. These differences are indicated in the logic diagrams by a dot or a cross in the circle or square (Figure 2). Both the chassis tabs containing the card in question and the Printed Circuit Manual, Cordwood Modules (Pub. No. 60042700) contain electronic schematics of these special variations.

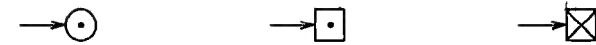


Figure 2. Special Inverters

Acceptable conventions for showing multiple inputs and outputs are given in Figure 3. Note that the output of inverter A is "0" only if inputs X, Y, and Z are all "1". The multiple outputs are identical.



Figure 3. Multiple Inputs/Outputs

Acceptable conventions for showing inverter networks are illustrated in Figure 4. As a general rule, circle inverters alternate with square inverters wherever possible. Because multiple outputs are identical, only one arrow is shown in cases where an inverter (A) serves as the single input to several succeeding inverters. In more complex inverter networks, multiple arrows are used (B to C and D; in this case because B is not the only input to C or D).

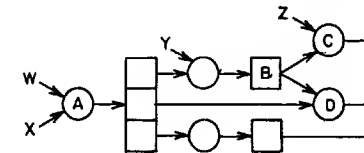


Figure 4. Inverter Networks

Test Points

A test point has no logic function, but is shown in the logic diagrams as a triangle (Figure 5). They are numbered from 1 to 6.



Figure 5. Test Point Symbols

*Registered trademark of Control Data Corporation

KEY TO LOGIC SYMBOLS (Cont.)

Flip-Flops (FF)

The flip-flop (FF) is a storage device with two stable states--designated as Set and Clear--and is composed of two inverters (Figure 6). The flip-flop is said to be set when the set output (B) is a "1", and clear when it is a "0". Note that the input (A) must be "0" to set the flip-flop and (C) must be "0" to clear it.

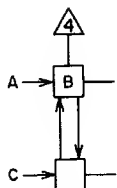


Figure 6. Flip-Flop Symbol

Logic signals are transmitted from one module to another by means of a line driver. Modules on the same chassis are connected with twisted pair lines, and those on separate chassis are connected by coaxial cable.

Twisted Pair Drivers

The twisted pair driver is represented by the standard square or circle. The output of the square or circle, however, is connected to a pin of the module in question and wired from there to a pin on another module (Figure 7). The ground wire of the pair is wired to the connector ground bus of each module. The pins are represented by small circles and are numbered from 1 to 28 (Pins 29 and 30 are ground and +6 volts, respectively, and generally are not shown in logic diagrams). The module location is shown above the card, and the module type is denoted in the upper right corner.

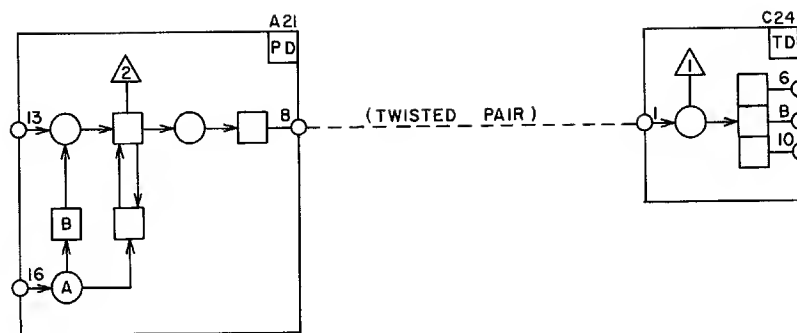


Figure 7. Twisted Pair Line Driver

Coaxial Cable Drivers

The coaxial cable driver is a 25 nsec pulse circuit, and is represented as shown in Figure 8. The pins used are represented by a small double circle.

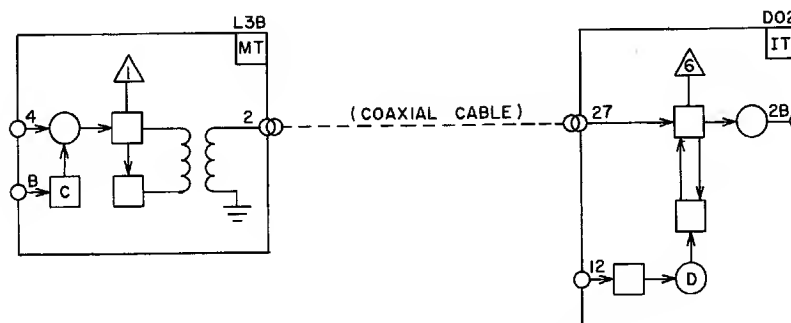


Figure 8. Coaxial Cable Driver

6600 COMPUTER I/O CHARACTERISTICS

GENERAL

The computer includes 10 separate Peripheral and Control Processors, any one of which can exchange data connected to 12 separate and identical data channels. Each external equipment communicates with the computer via a controller. A controller changes the one-shot pulse signals used by the computer into the signals required by the particular external equipment and vice-versa.

CHANNEL CHARACTERISTICS

Each channel handles 12-bit words at varying rates up to a maximum of one word every usec, the equivalent of a one megacycle (mc) transfer rate. All channels may be in operation at the same time.

Pulse communication is used on all the data and control lines of a channel, and all lines are synchronized to the processor clock system.

Each channel has a 12-bit bi-directional register plus several bi-directional control designators which define the status of the register and the channel.

A channel active designator (flag) is set from an internal source to reserve a channel for communication between a processor and controller. A channel inactive signal from an internal or external source clears the channel active flag to terminate communication.

A channel full flag is set at the same time a word is entered in the channel register from internal or an external source. An internal or external channel empty signal clears the full flag, which in turn clears the channel register.

The pulses on the data and control lines are one shot, non-repeated type transmissions, and all controllers must provide for storing the information.

Other control includes two clock signals and one master clear signal for external devices. Clock signals are 10 mc (100 nsec period) and 1 mc usec period.

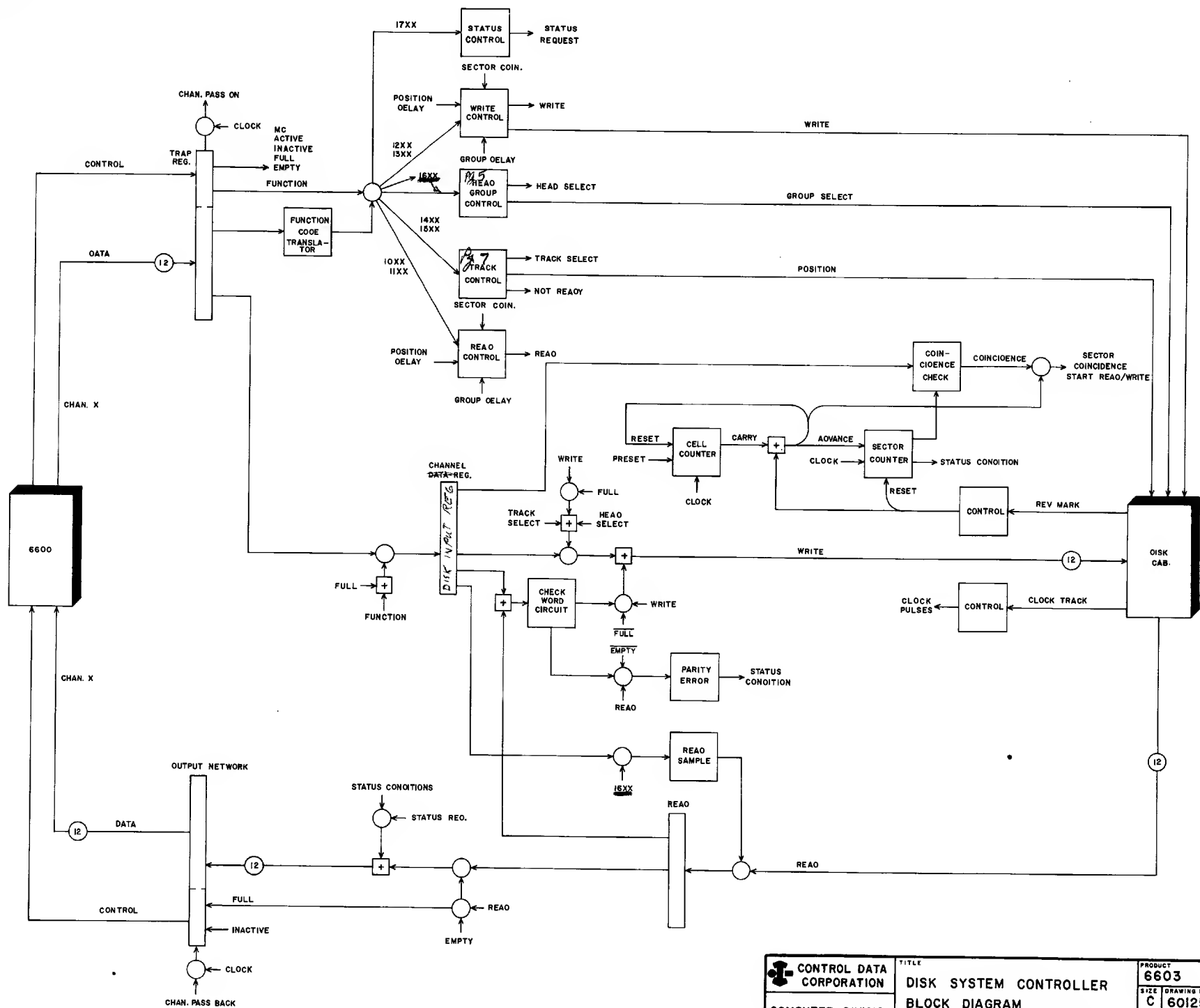
Channel data and control lines are grouped into two cables, input and output (Fig. 2). The output cable carries processor signals to controllers; the input cable carries controller signals to the processor and also carries the two processor clock signals to controllers.

All devices on a channel connect to the data and control lines in a series-parallel scheme. Each controller samples the lines and unconditionally relays all signals to the next in-line controller (which may be the processor). Each controller times the signal relay on the 10 mc clock signal from the processor so all controllers and the processor are synchronous and time displaced from each other one or more clock periods. The scheme provides for orderly, high-speed data exchange. For further information see 6600 I/O Specs. Pub. No. 60045100.

6603 DISK SYSTEM CONTROLLER

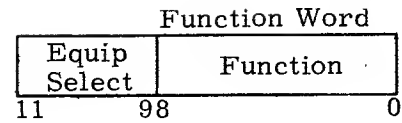
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15	Read Control		
16	Read Sequence		
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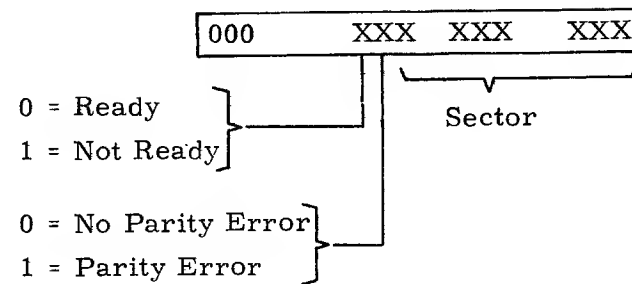
DISK SYSTEM CONTROLLER

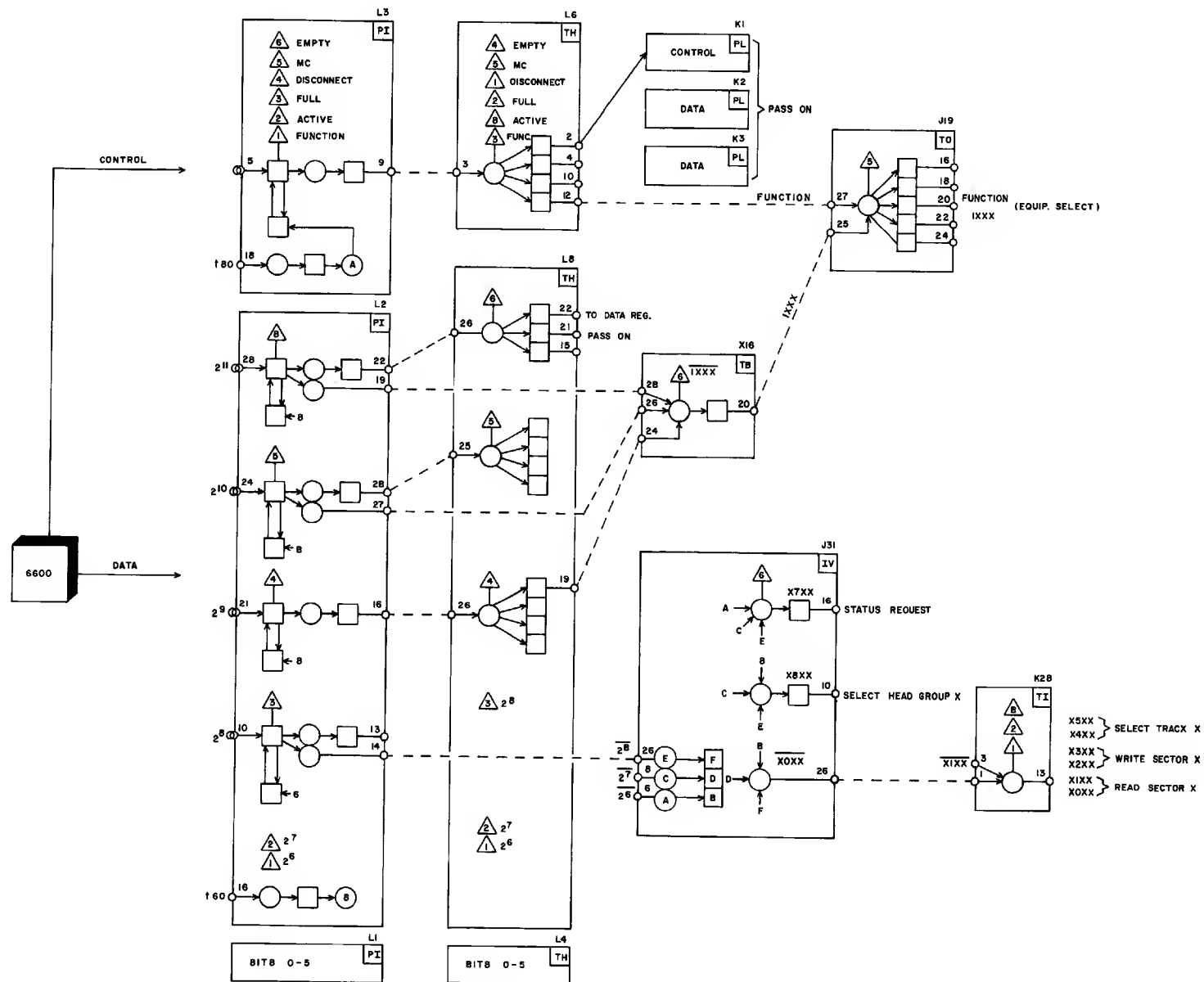
FUNCTION CODES

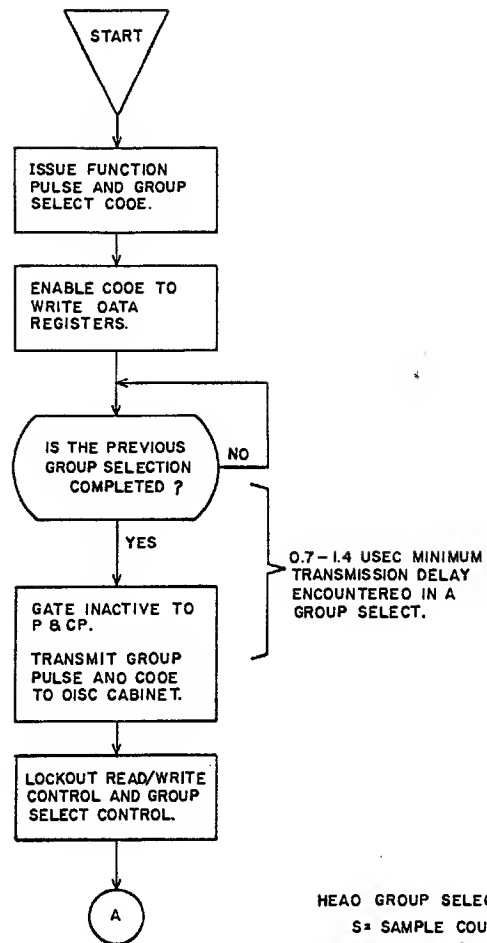


S0xx - S1xx Read Sector X
 S2xx - S3xx Write Sector X
 S4xx - S5xx Select Track X
 S60x Select Head Group X
 S700 Status Request

Status Reply Word

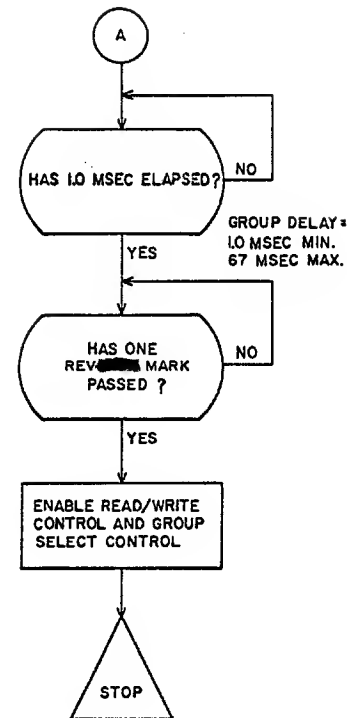






HEAD GROUP SELECT CODE - 16SG
 S= SAMPLE COUNT CONTROL
 G= HEAD GROUP

FLOW CHART
HEAD GROUP SELECT



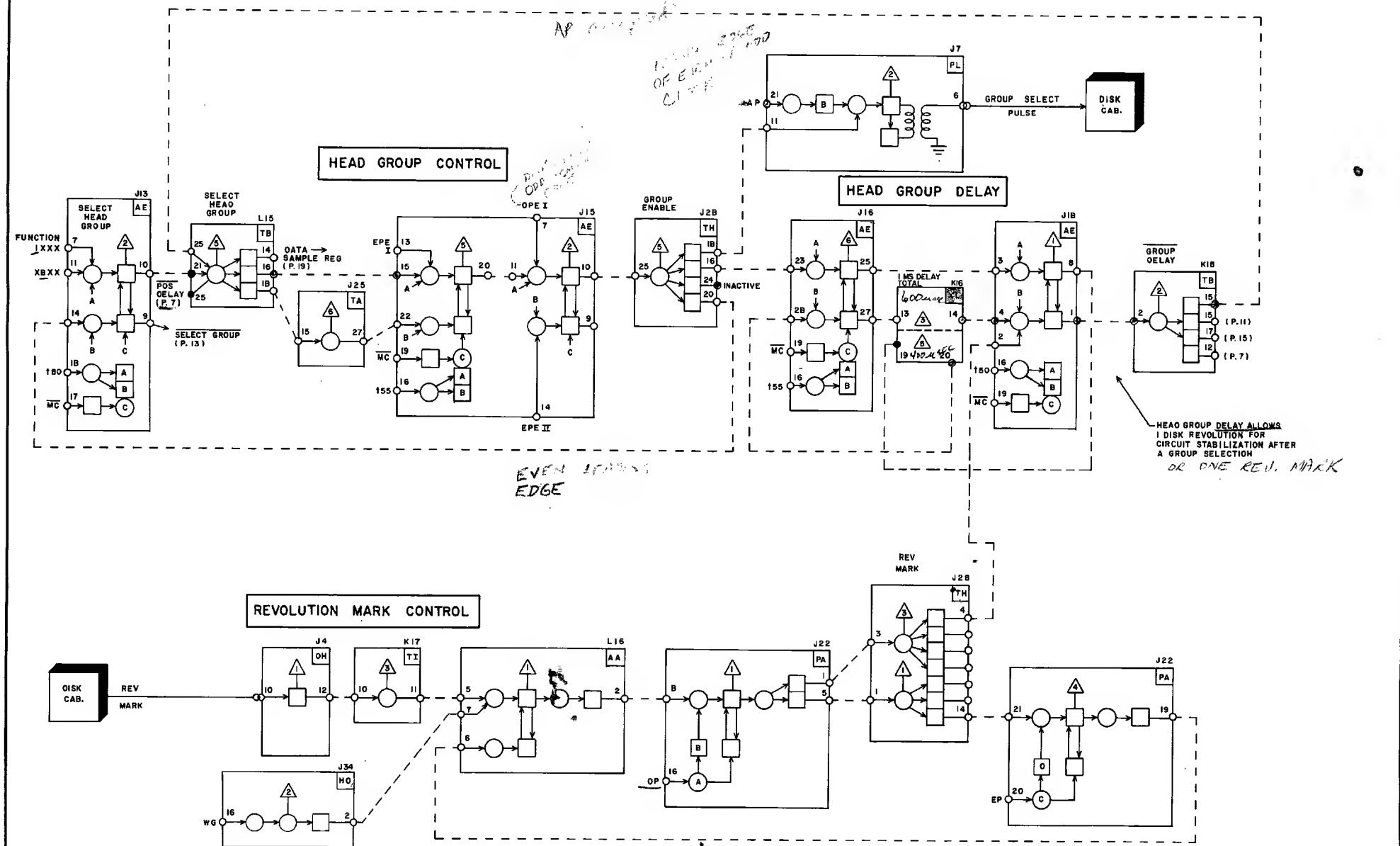
clock

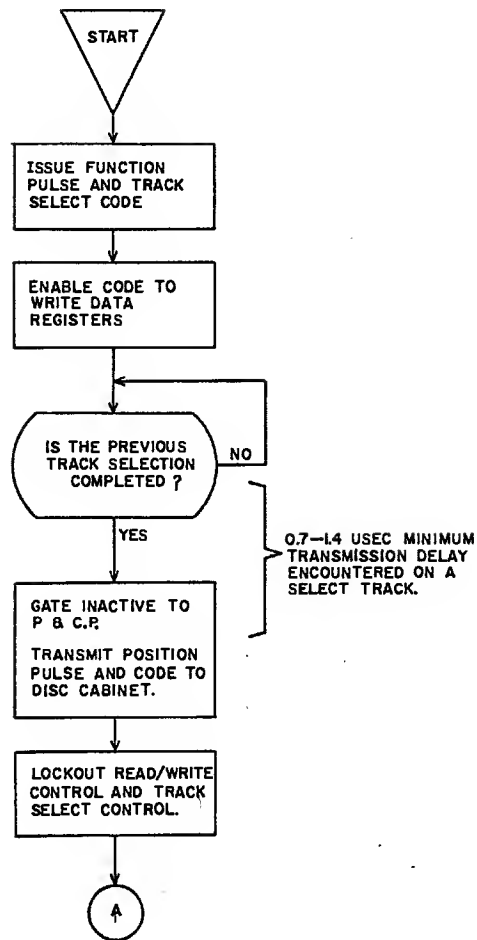
AP 11

EP 11

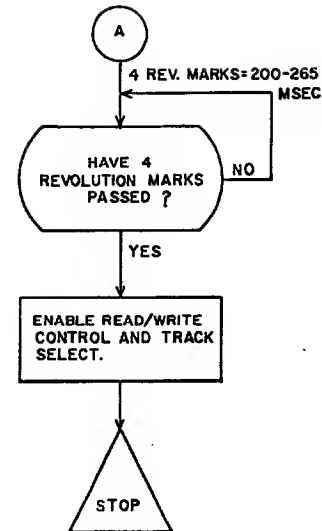
OP 11

*AP sample
 EP sample
 OP odd*



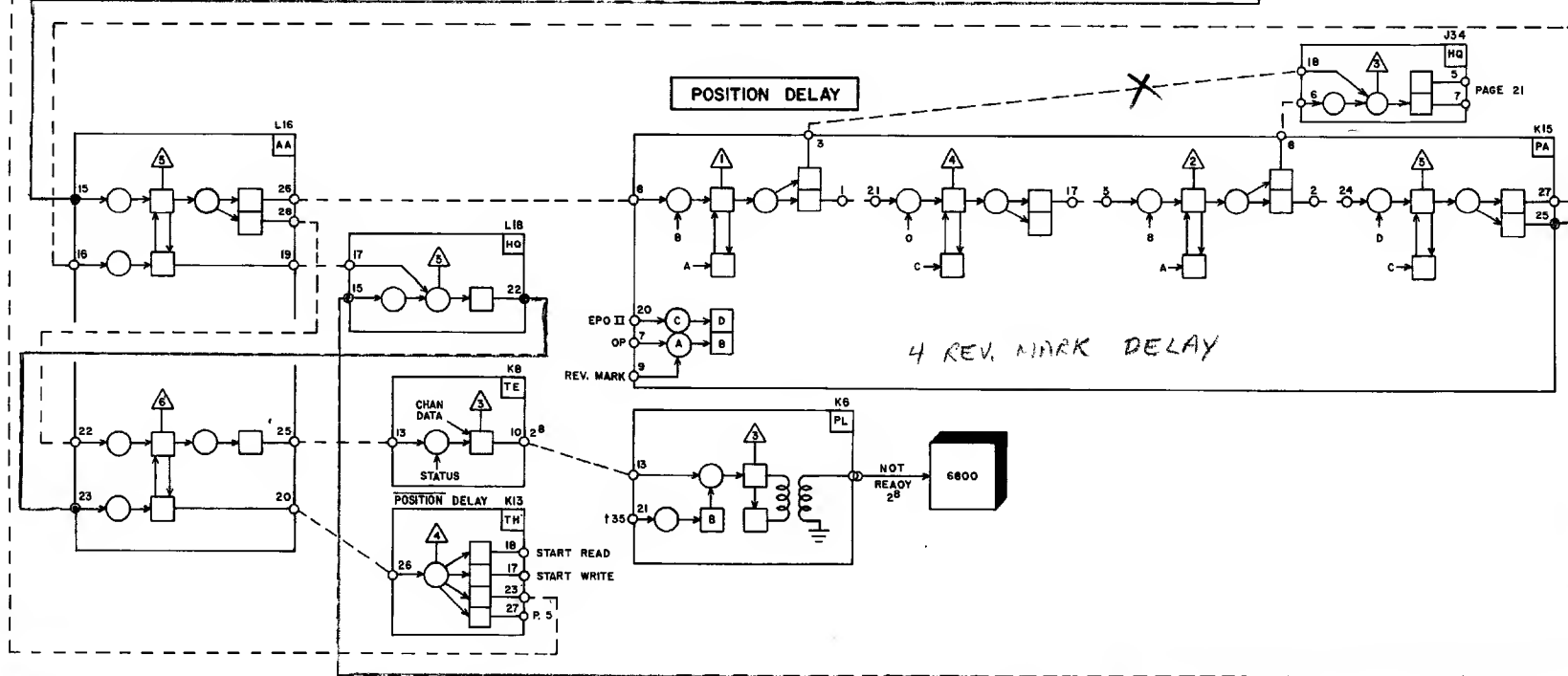
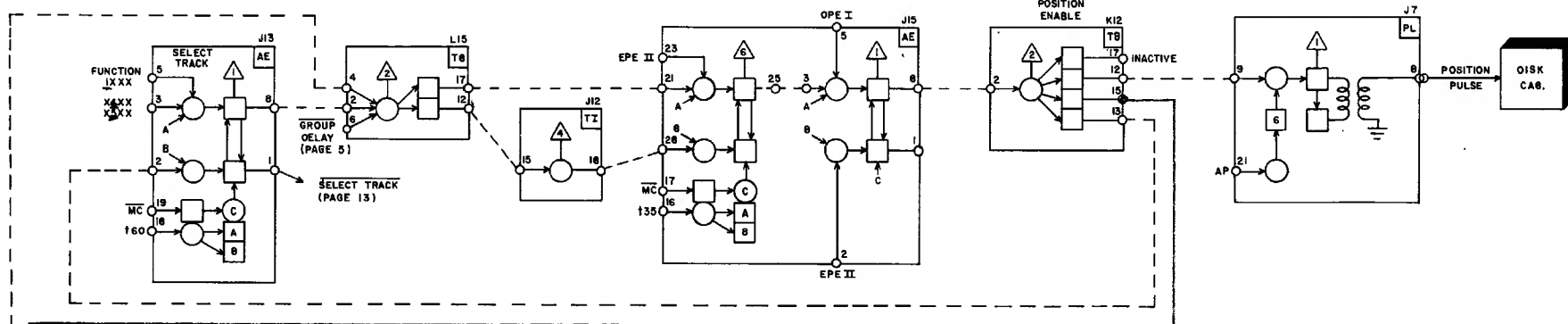


TRACK SELECT CODES:
 14XX = TRACKS 000-077
 15XX = TRACKS 100-177



FLOW CHART
TRACK SELECT

TRACK CONTROL



POSITION DELAY ALLOWS DISK HEADS TO RE-POSITION AND STABILIZE FOR 4 DISK REVOLUTIONS BEFORE ALLOWING READ/WRITE TO START. SEE READ/WRITE CONTROL DWGS.

CELL COUNTER

The 9-bit cell counter is synchronized with disk rotation by the disk clock and is advanced every 1.4 μ sec (outer two disk zones) or 1.8 μ sec (inner two disk zones). Upon a carry out of the cell counter (count = 777₈) and coincidence of sector address with sector count, the Read/Write is enabled. The counter is reset to 240₈ to obtain a count of 352₁₀ cells.

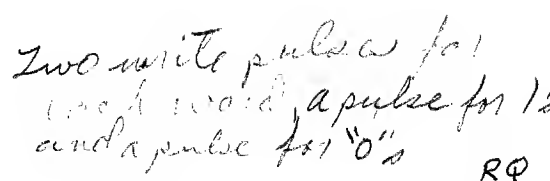
SECTOR COUNTER

This 8-bit counter is also synchronized with the disk; it is advanced with a carry out of the cell counter. For the two outer zones (1.4 μ sec clock) it counts

128₁₀ sectors, and for the inner zones (1.8 μ sec clock) it counts 100₁₀ sectors. This counter is reset to 377₈ by the disk revolution mark.

COINCIDENCE CHECKER

Upon placement of a sector address in the channel register, the coincidence checker compares it with the sector count. When the two are equal, the disk is at the start of the selected sector and the Read or Write is enabled.



3.5, 4.2, 4.9, 5.6, 6.3, 7.0, 7.7, 8.4, 9.1, 9.8, 10.5

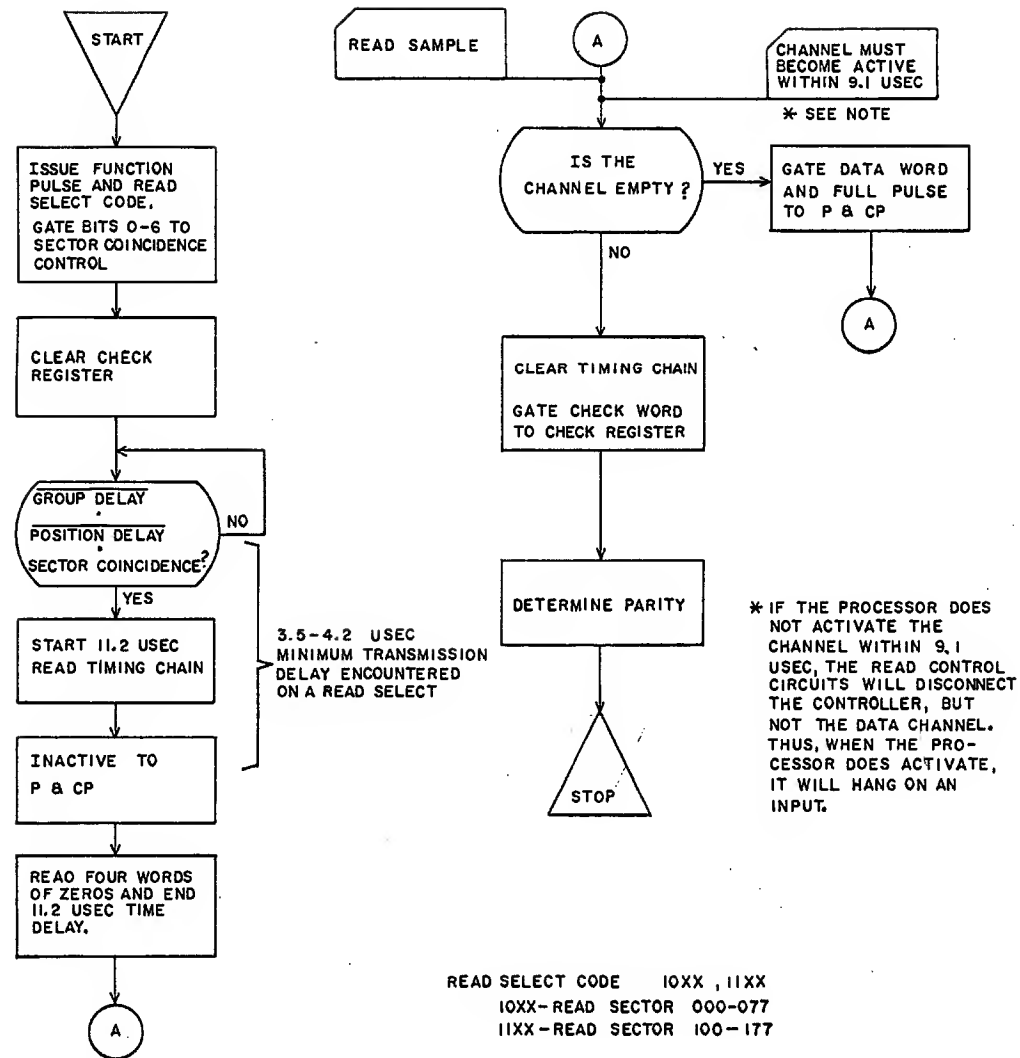
1st half of 1st OP
2nd half of 1st OP
1st half of 2nd OP
2nd half of 2nd OP
1st half of 3rd OP
2nd half of 3rd OP
1st half of 4th OP
2nd half of 4th OP
1st half of 5th OP
2nd half of 5th OP

4. 5. 6. 7. 8. 9. 10.

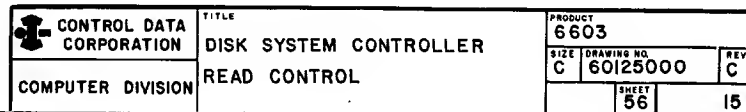
WRITE SEQUENCE

The processor sends data to an external device in the following manner:

1. The processor places a function word in the channel register and sets the full flag and the channel active flag. Coincidentally, it sends the word and a function signal to all devices. The function signal tells all controllers to sample the word and identifies the word as a function code rather than a data word. The code selects a controller and a mode of operation. Non-selected controllers clear, leaving only the selected one turned on.
2. The controller sends an inactive signal to the processor, indicating acceptance of the function code. The signal drops the channel active flag which in turn drops the full flag and clears the channel register.
3. The processor sets the channel active flag and sends an active signal to the controller which signals the device that data flow is starting.
4. The processor places a data word in the channel register and sets the full flag. Coincidentally, it sends the word and a full signal to the controller.
5. The controller accepts the word and sends an empty signal to the processor where it clears the channel register and drops the full flag.
6. Steps 4 and 5 repeat for each processor word.
7. After the last word is transferred and acknowledged by the controller empty signal, the processor drops the channel active flag and sends an inactive signal to the controller to turn it off.



FLOW CHART
DISC READ OPERATION



READ SEQUENCE

An external device sends data to the processor by way of the controller in the following manner.

1. The processor places a function word in the channel register and sets the full flag and the channel active flag. Coincidentally, it sends the word and a function signal to all controllers. The function signal tells all controllers to sample the word and identifies the word as a function code rather than a data word. The code selects a controller and a mode of operation. Non-selected controllers clear, leaving only the selected one turned on.
2. The controller sends an inactive signal to the processor indicating acceptance of the function code. The signal drops the channel active flag which in turn drops the full flag and clears the channel register.
3. The processor sets the channel active flag and sends an active signal to the controller which signals the device to start sending data.
4. The device reads a word and then sends the word to the channel register with a full signal which sets the channel full flag.
5. The processor stores the word, drops the full flag, and returns an empty signal indicating acceptance of the word. The device clears its data register and prepares to send the next word.
6. Steps 4 and 5 repeat for each word transferred.
7. At the end of the transfer, the controller clears its active condition and sends an inactive signal to the processor to indicate end of data. The signal clears the channel active flag to disconnect the controller and the processor from the channel.
8. As an alternative, the processor may choose to disconnect from the channel before the

device has sent all of its data. The processor does this by dropping the active flag and sending an inactive signal to the controller which immediately clears its active condition and sends no more data, although the device may continue to the end of its data record or cycle.

STATUS REQUEST

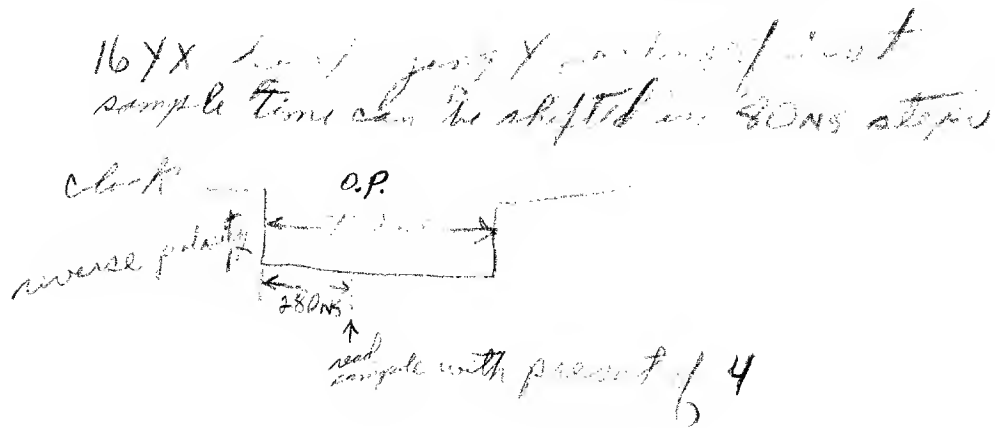
A status request is a special one word data input transfer in which an external device indicates a ready or error condition to a processor.

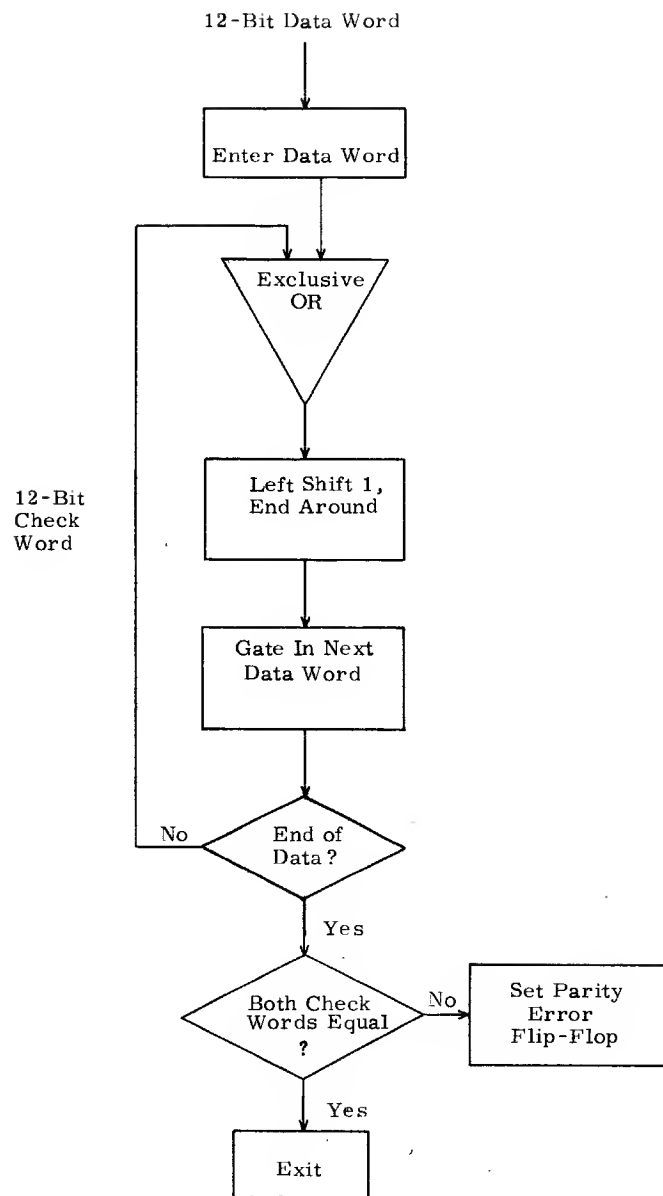
1. The processor places a function word in the channel register and sets the full flag and the channel active flag. Coincidentally, it sends the word and a function signal to all controllers. The function signal tells all controllers to sample the word and defines the word as a function code rather than a data word. The code selects a controller and places it in status mode. Non-selected controllers clear, leaving only the selected one turned on.
2. The controller sends an inactive signal to the processor indicating acceptance of the status function code. The signal drops the channel active flag which in turn drops the full flag and clears the channel register.
3. The processor sets the channel active flag and sends an active signal to the controller which signals the device to send the status word.
4. The controller sends the status word to the channel register with a full signal which sets the channel full flag.
5. The processor stores the word, drops the full flag, and returns an empty signal indicating acceptance of the word.
6. The processor drops the channel active flag to disconnect the channel and sends an inactive signal to the controller to disconnect it.

READ SAMPLE

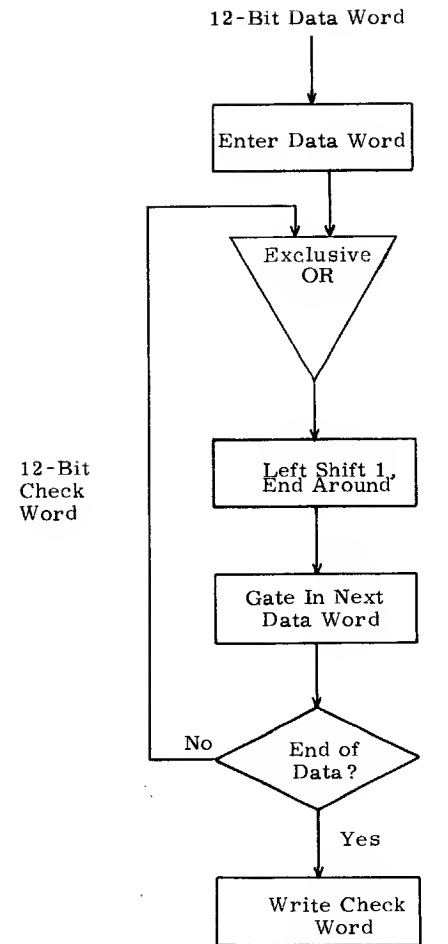
The Read Sample circuit allows the programmer to vary the time at which disk data is sampled during a Read operation. This is accomplished by presetting a 3-bit counter which produces the desired delay before sending a Clear/Set

sampling pulse to the data input register. By changing the preset count, the sample pulse can be varied in 80 to 90 nsec intervals over a range of about 700 nsec. Normal sampling is when $Y=0$ in the head group select code 16 YX.



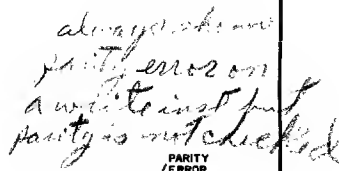


READ CHECK WORD



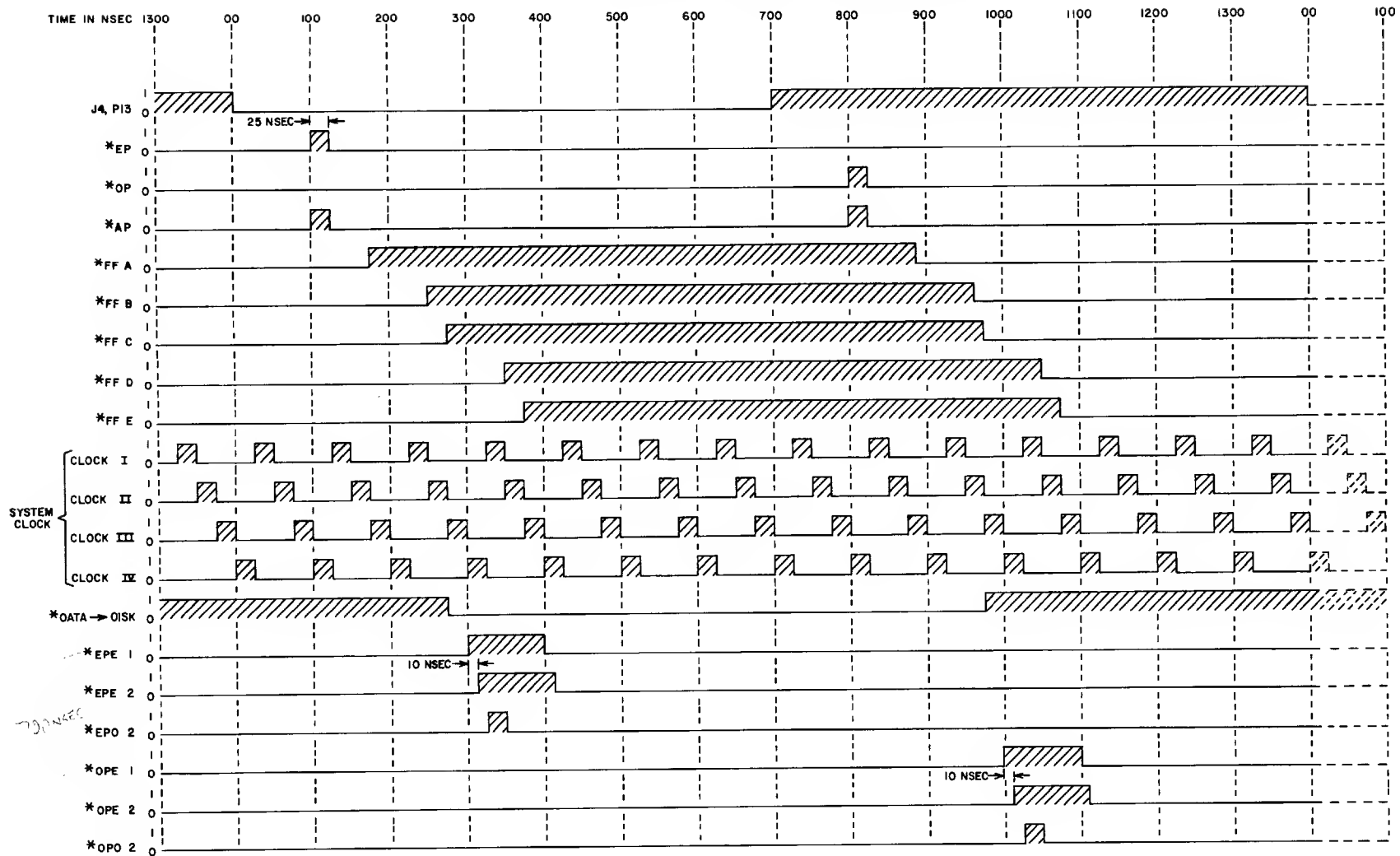
WRITE CHECK WORD

Check word is the total of binary input bits left shifted each time a word is written then the complement of this check word then has every other bit complemented then written on the disk



NOTE: BITS 1, 3, 5, 7, 9, AND 11 OF THE CHECK WORDS ARE COMPLEMENTED WHEN IT IS WRITTEN ON THE DISK. WHEN THE CHECK WORDS ARE COMPARED DURING READ IT THEN LOOKS FOR 5252₈ AT K27.

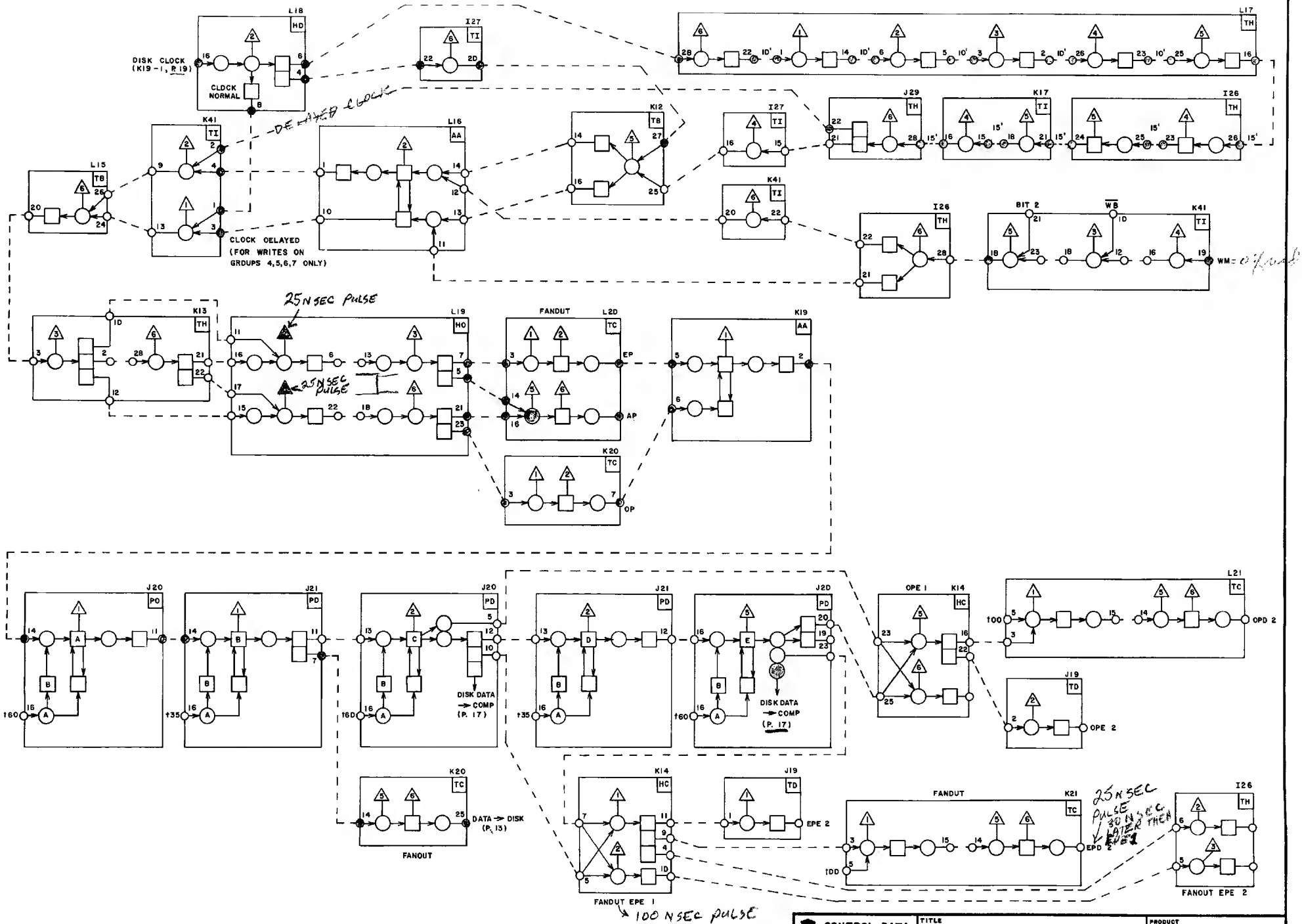
CLOCK CONTROL TIMING CHART



NOTE:

THE FORMATION OF OPE 1 & OPE 2 CLOCK PULSES IS SHOWN AS AN AVERAGE AND DEPENDS ON THE DISK TO COMPUTER CLOCK RELATIONSHIP.

*TIMING SHOWN IS FOR A READ OPERATION, OR A WRITE IN GROUPS 0 THRU 3. FOR WRITING IN GROUPS 4 THRU 7, THESE SIGNALS ARE DELAYED APPROX. 300 NANoseconds.



CONTROL DATA
CORPORATION

COMPUTER DIVISION

TITLE

DISK SYSTEM CONTROLLER
CLOCK CONTROL

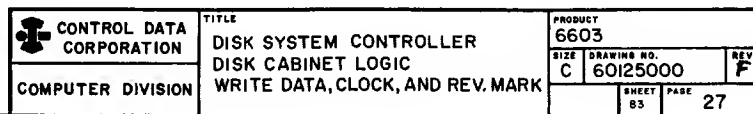
PRODUCT
6603

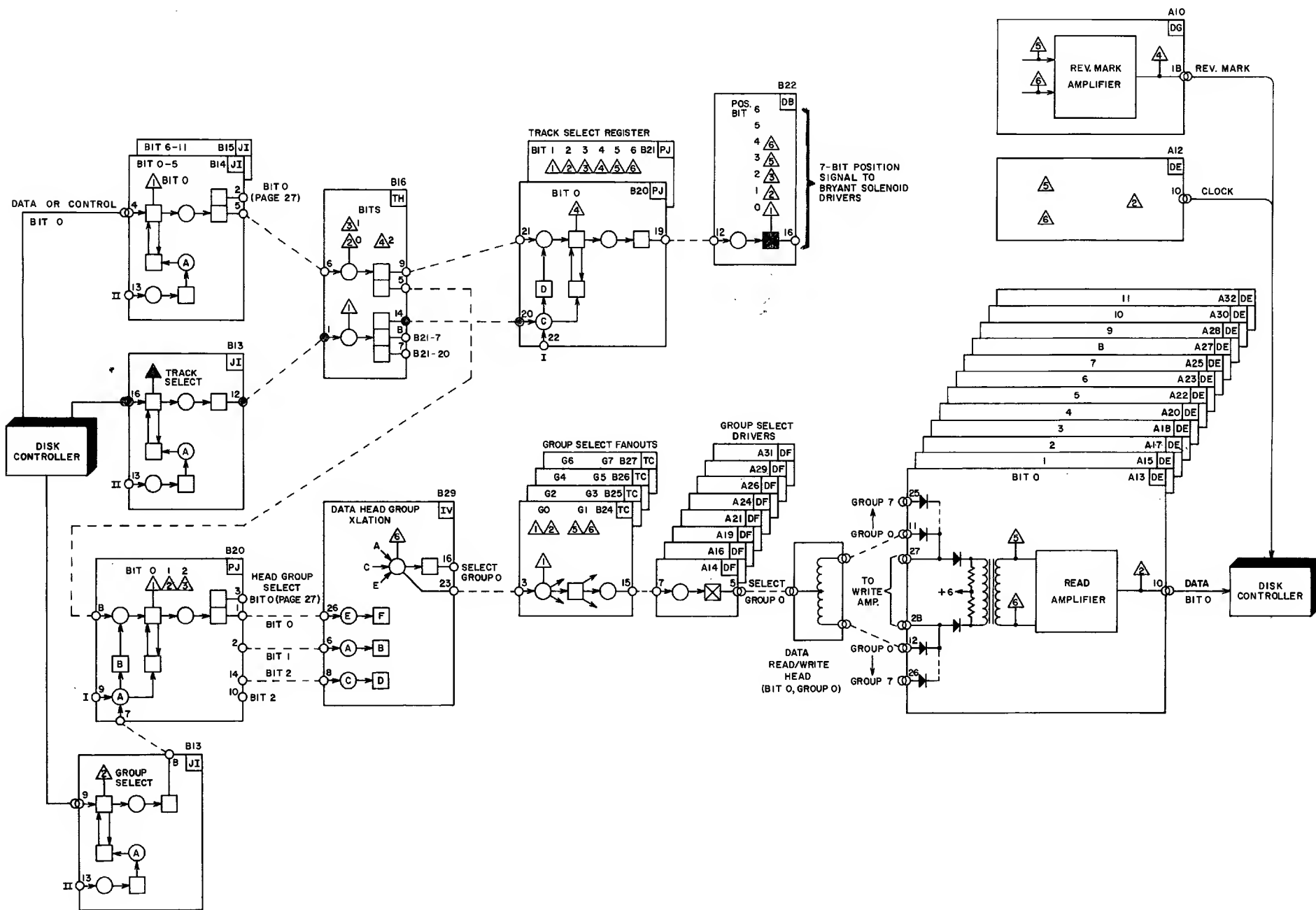
SIZE DRAWING NO.
C 60125000

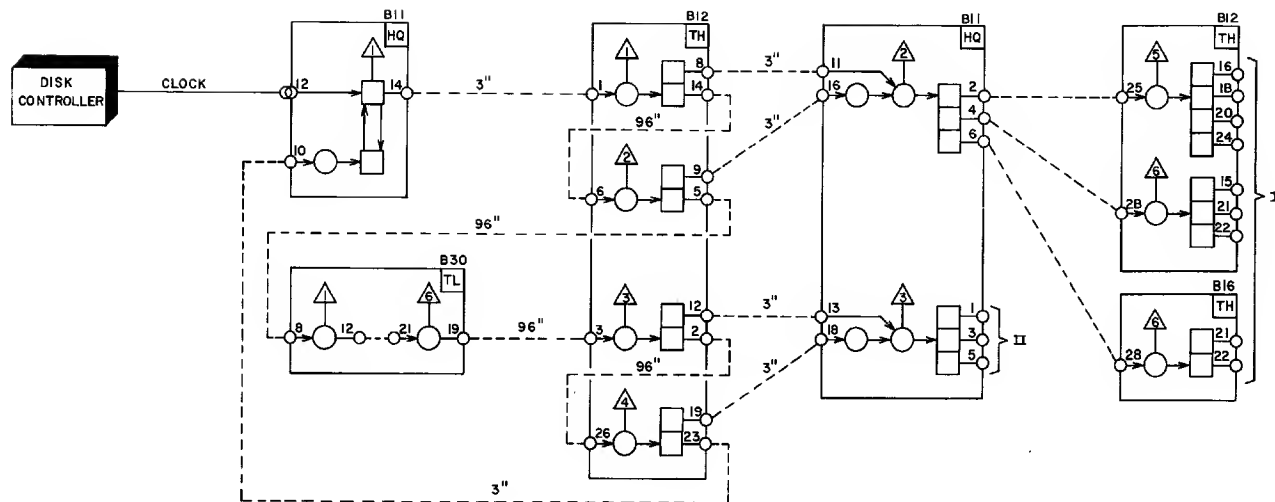
REV
F

SHEET
60

PAGE
25



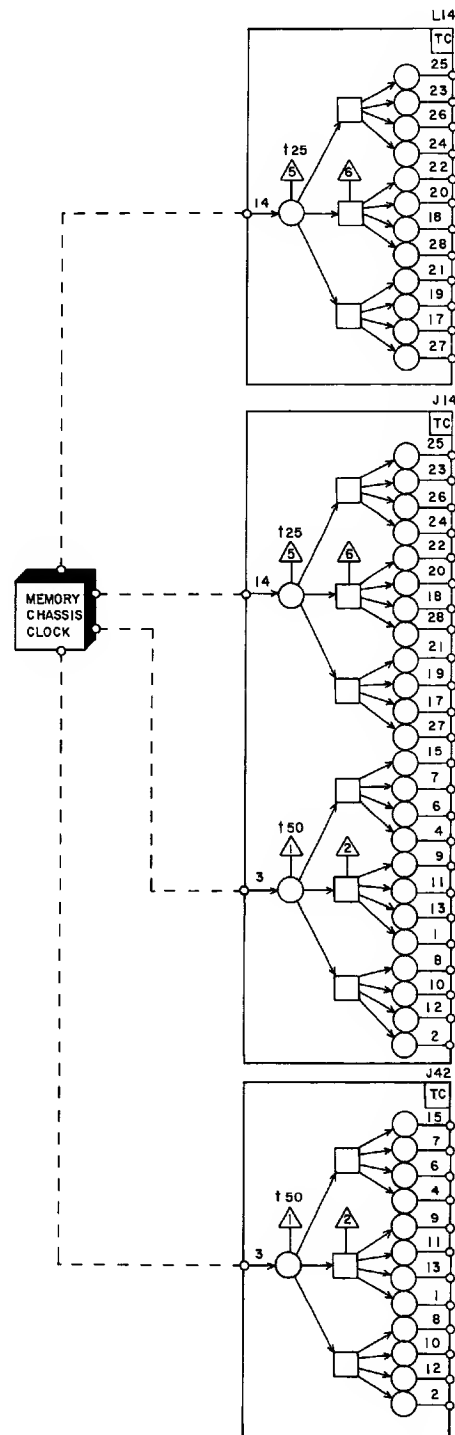





CONTROL DATA CORPORATION
COMPUTER DIVISION

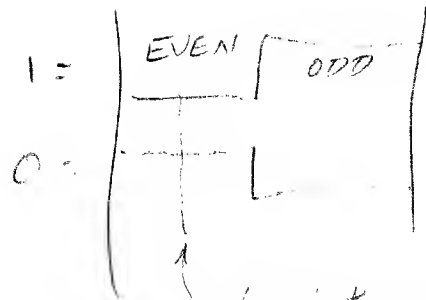
TITLE
DISK SYSTEM CONTROLLER
DISK CABINET LOGIC
CLOCK

PRODUCT 6603		REV F
SIZE C	DRAWING NO. 60125000	
SHEET 85	PAGE 30.1	

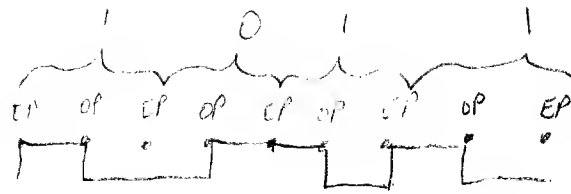


	CONTROL DATA CORPORATION	TITLE DISK SYSTEM CONTROLLER CLOCK	PRODUCT 6603		
	COMPUTER DIVISION		SIZE C	DRAWING NO. 60125000	REV C
			SHEET 63		31

1 clock period

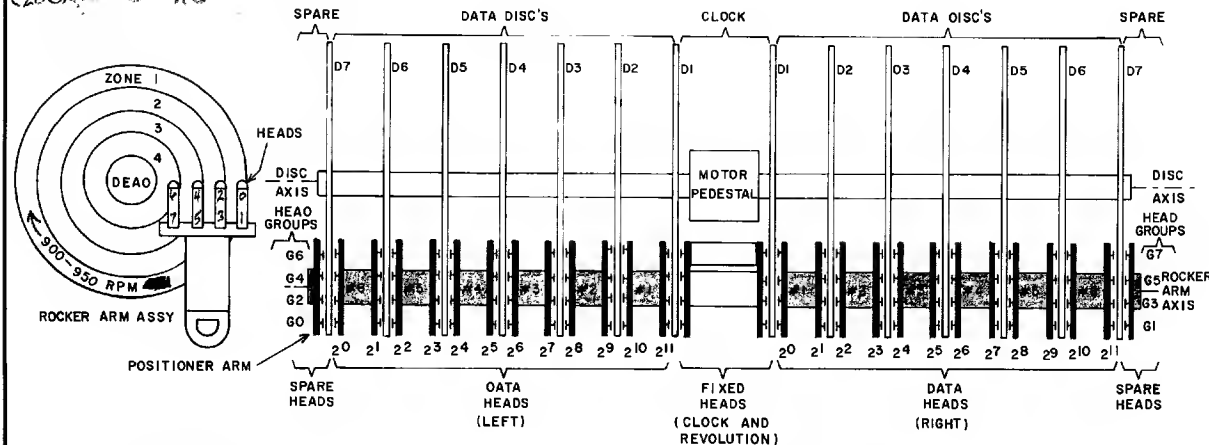


mid point may be varied 70 mm on either side of center



Calderon - 22 of 100. 100. 100.

CLOCK DISC REVOLUTION



RECORDING SCHEME
1 BIT/SECTOR IN 12 PARALLEL SECTORS LOCATED ON 12 DISC SURFACES IN THE ODD HEAD GROUP (RIGHT OF PEDESTAL) OR THE EVEN HEAD GROUP (LEFT OF PEDESTAL). TOTAL SECTORS - 116,736.

TOTAL BITS - 486,088,704
(116,736 SECTOR X 347 WORDS X 12 BITS)
448,766,240 (116,736 X 320 X 12)
TOTAL PP WORDS (12 BIT) = 37,355,520
TOTAL CP WORDS (60 BIT) = 7,471,104

6 DATA DISKS (EVEN HEAD GROUPS 0, 2, 4, 6)

6 DATA DISKS (ODD HEAD GROUPS 1, 3, 5, 7)

REV. MARK/CLOCK TRACK DISKS

MOTOR PED.

128 TRACKS PER HEAD

128 SECTORS

CLOCK = 1.4 μSEC

750 KC

100 SECTORS

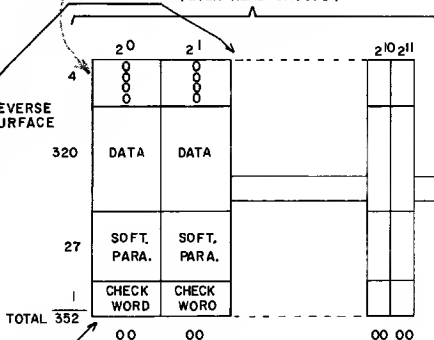
CLOCK = 1.8 μSEC

600 KC

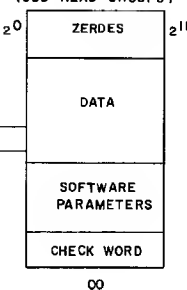
900 RPM
EXPECTED RANDOM ACCESS = 33 MILLISEC

3 unusable sectors (group switch gap)

12 DISK SURFACES (EVEN HEAD GROUPS)



12 DISK SURFACE (ODD HEAD GROUPS)



$$8 \times 128_{10} = \text{TRACKS}$$

$$4 \times 128_{10} \times 128_{10} = \text{SECTORS IN OUTER ZONE} = 65536$$

$$4 \times 128 \times 100 = \text{SECTORS IN INNER ZONE} = 51200$$

$$512_{10} = \text{CM. WORDS PER SECTOR}$$

$$2560_{10} = \text{PPU WORDS PER SECTOR}$$

351 WORDS PER SECTOR

37,355,520 WORDS MAY BE WRITTEN ON THE DISKS.

* GROUP DELAY BETWEEN HEAD SELECTION IS FROM 1 millisecc to 67 millisecc (1 new mark)

* track selection delay is (4 new marks) at a minimum of 201 millisecc to a maximum of 268 millisecc figured on change from track 1 to track 128.

tracks are .015 inches wide

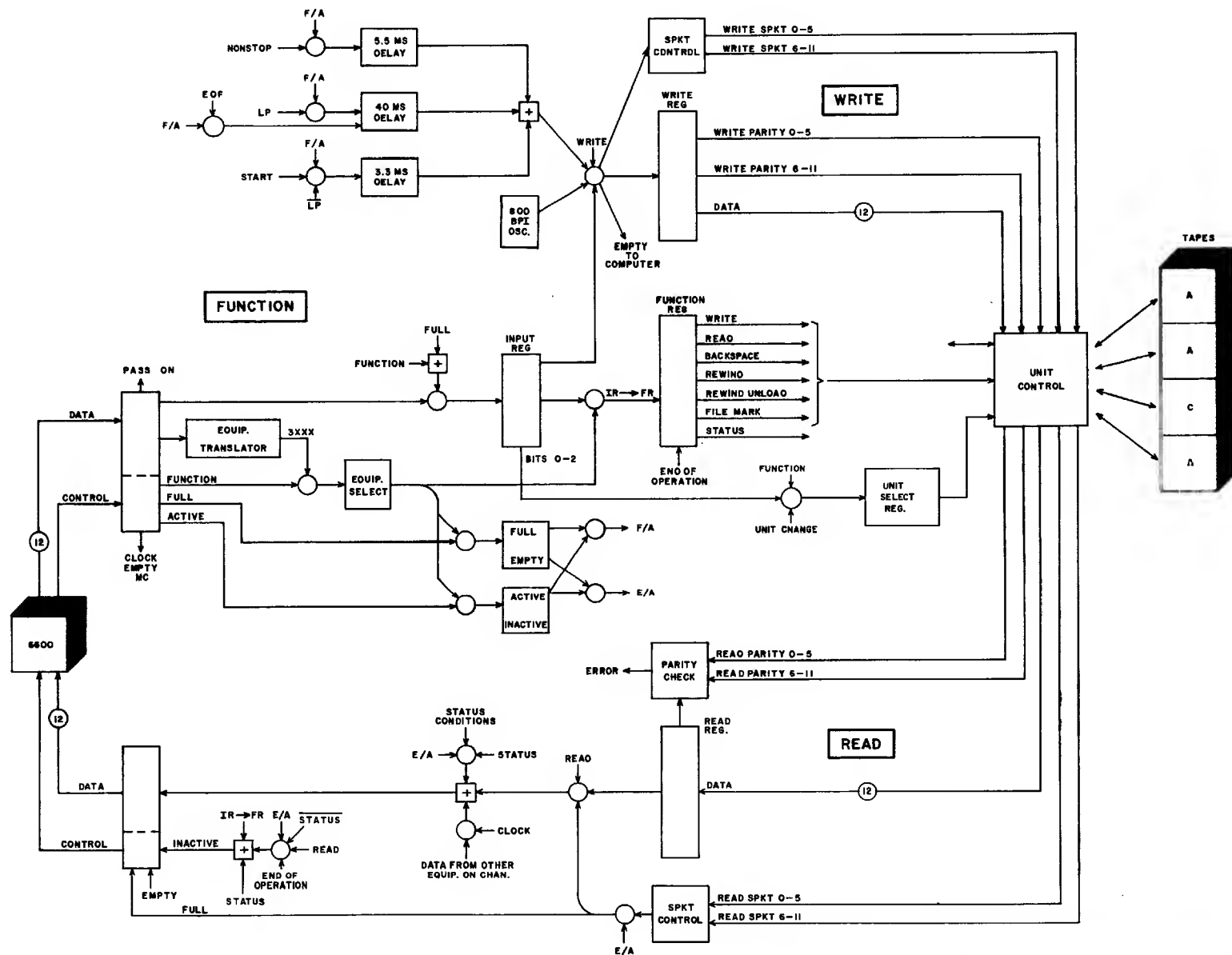
1 is written at even phase

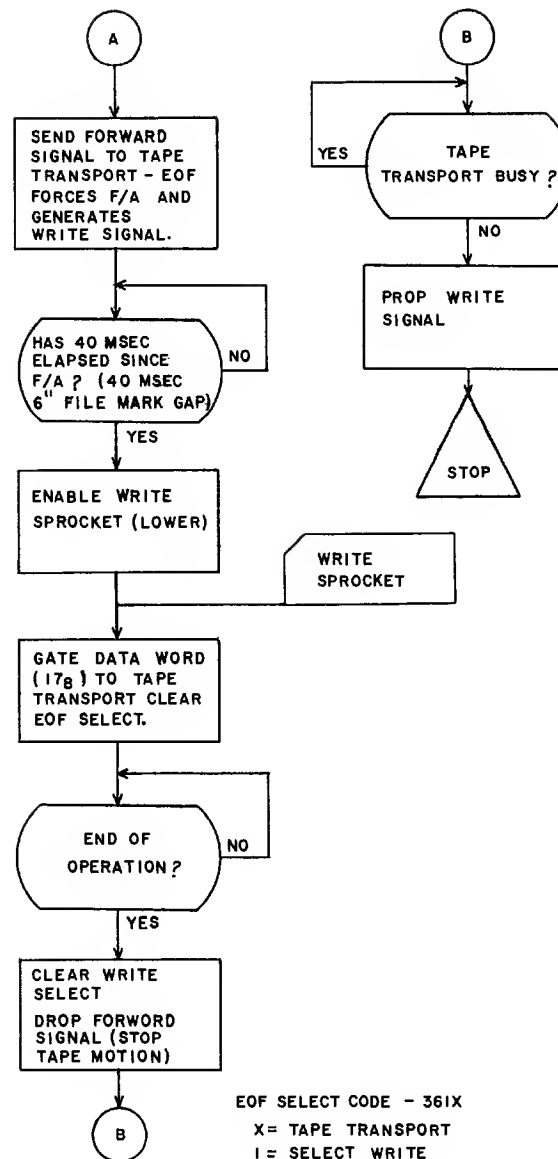
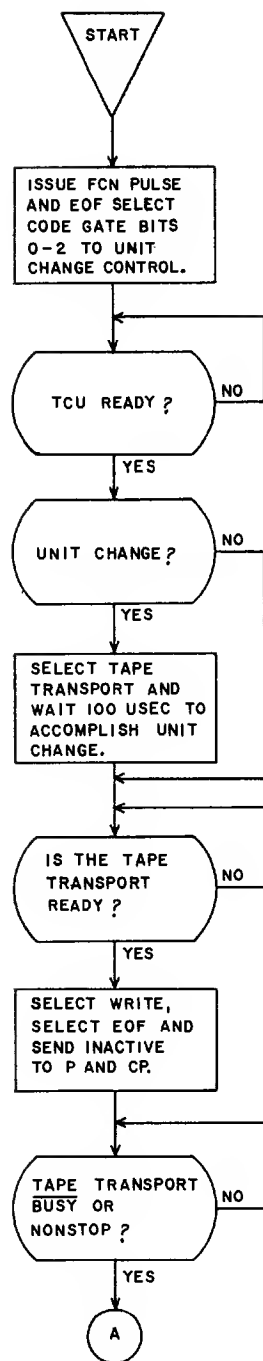
0 is written at odd phase

6622 MAGNETIC TAPE TRANSPORT CONTROLLER

CONTENTS

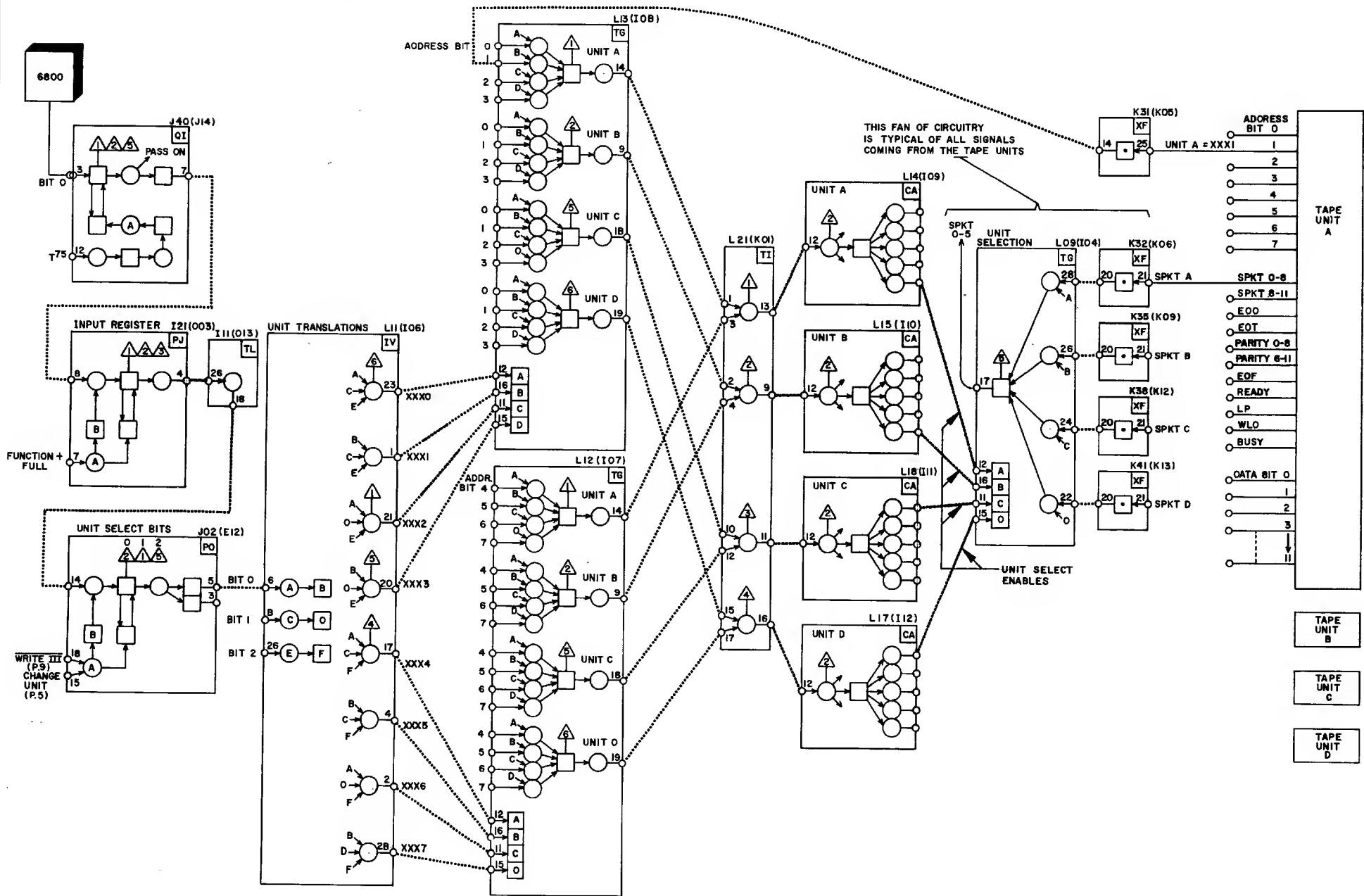
Page	Title
1	Block Diagram
2	End of File
3	Function Circuits I
5	Function Circuits II
7	Unit Control
8	Rewind Operation
9	Motion Control
11	Write Osc.
12	Tape Read Operation
13	Write Data Flow
15	Read Sprocket Control
16	Tape Read Operation
16. 1	Read Parity Checking Circuits
17	Read Data Flow
19	Status Circuits
21	Non-Stop, End of Operation, Busy/Ready
23	Clock (Freon-Cooled Controllers)
25	Clock (Air-Cooled Controllers)





EOF SELECT CODE - 361X
 X = TAPE TRANSPORT
 1 = SELECT WRITE
 6 = SELECT EOF
 3 = SELECT EQUIPMENT

FLOW CHART
 END OF FILE



NOTE:

MODULE LOCATIONS IN PARENTHESIS
ARE FOR AIR COOLED 6622 TAPE
CONTROLLERS.

CONTROL DATA
CORPORATION

COMPUTER DIVISION

TITLE

TAPE TRANSPORT CONTROLLER
UNIT CONTROL

PRODUCT

6622-A/B

SIZE DRAWING NO.

C 60125000

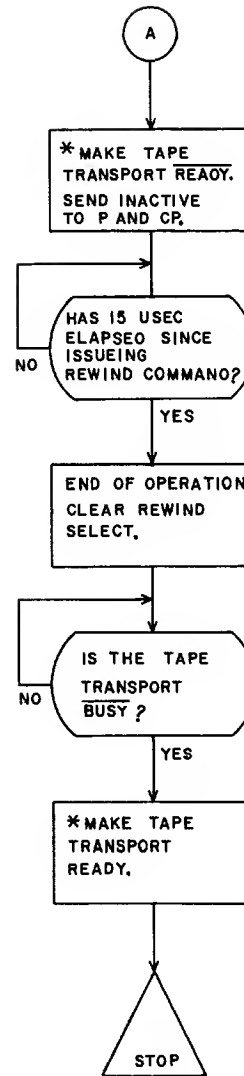
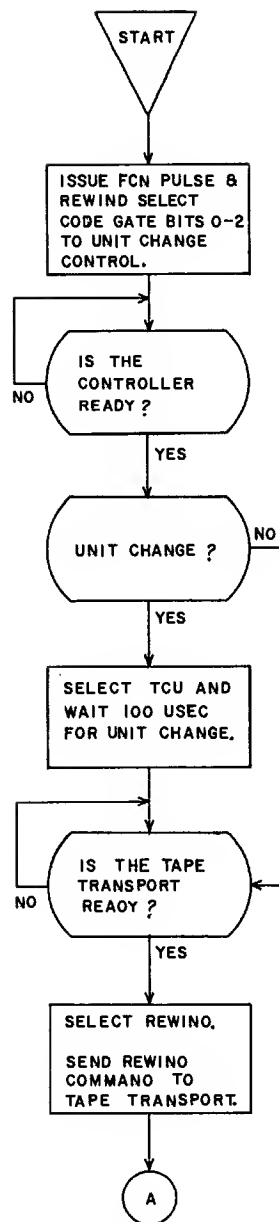
REV

N

SHEET

19

7

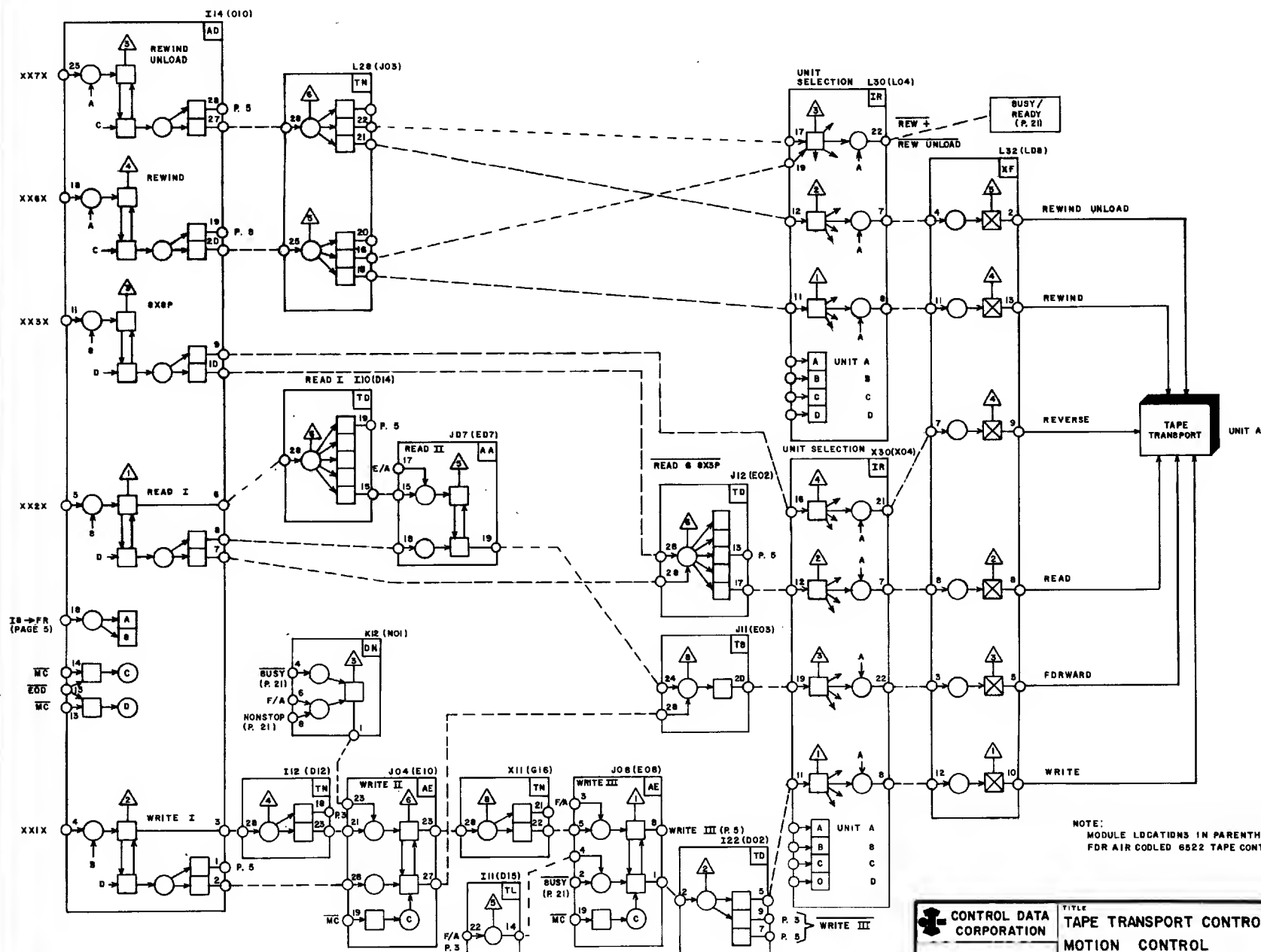


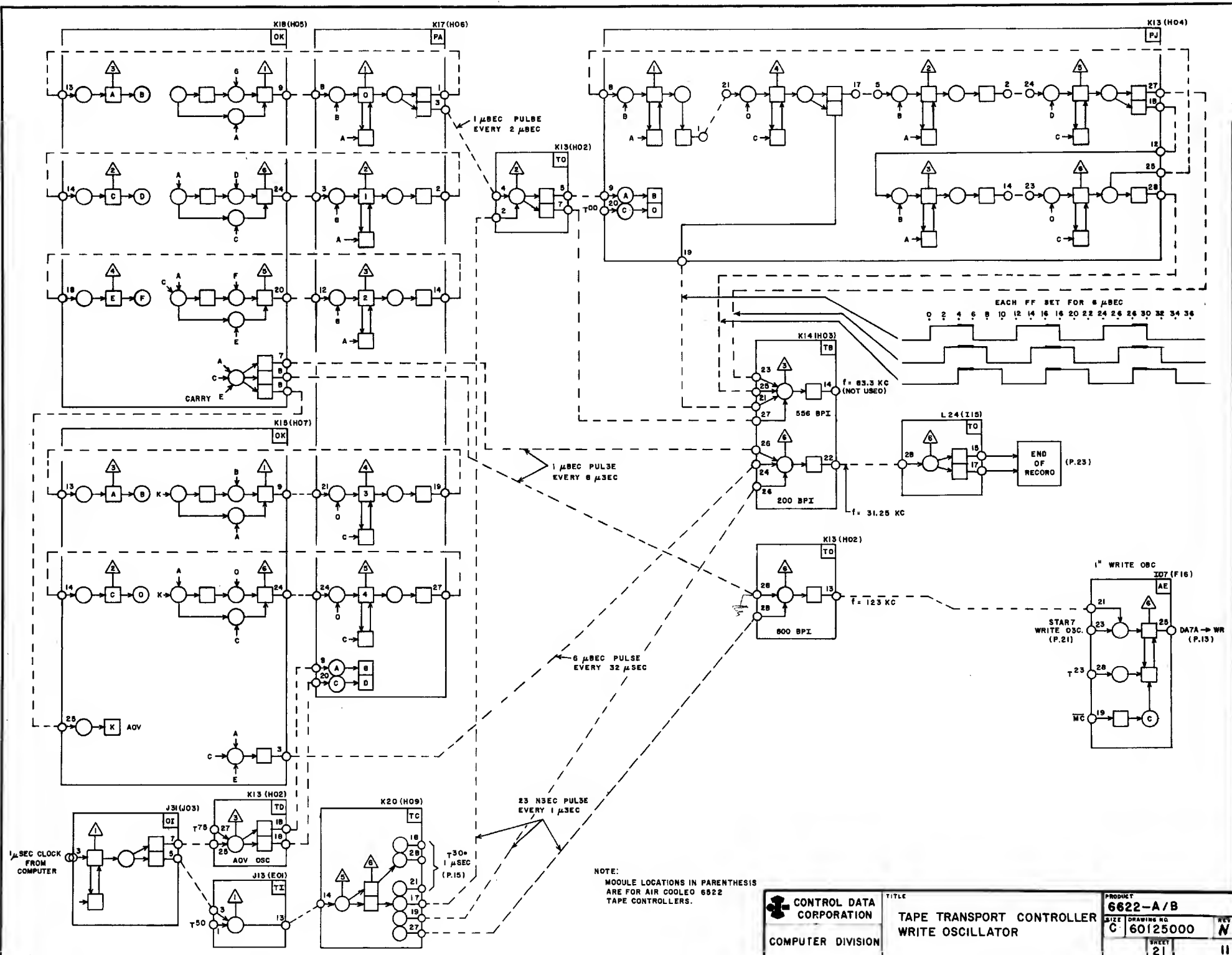
TAPE REWINDS UNDER ITS OWN CONTROL.

* TCU READY PREVENTS ANOTHER TAPE OPERATION FROM BEING INITIATED ON THE SAME TAPE UNIT UNTIL THE REWIND HAS BEEN COMPLETED.

REWIND SELECT CODE - 306X
X = TAPE TRANSPORT

FLOW CHART
REWIND OPERATION

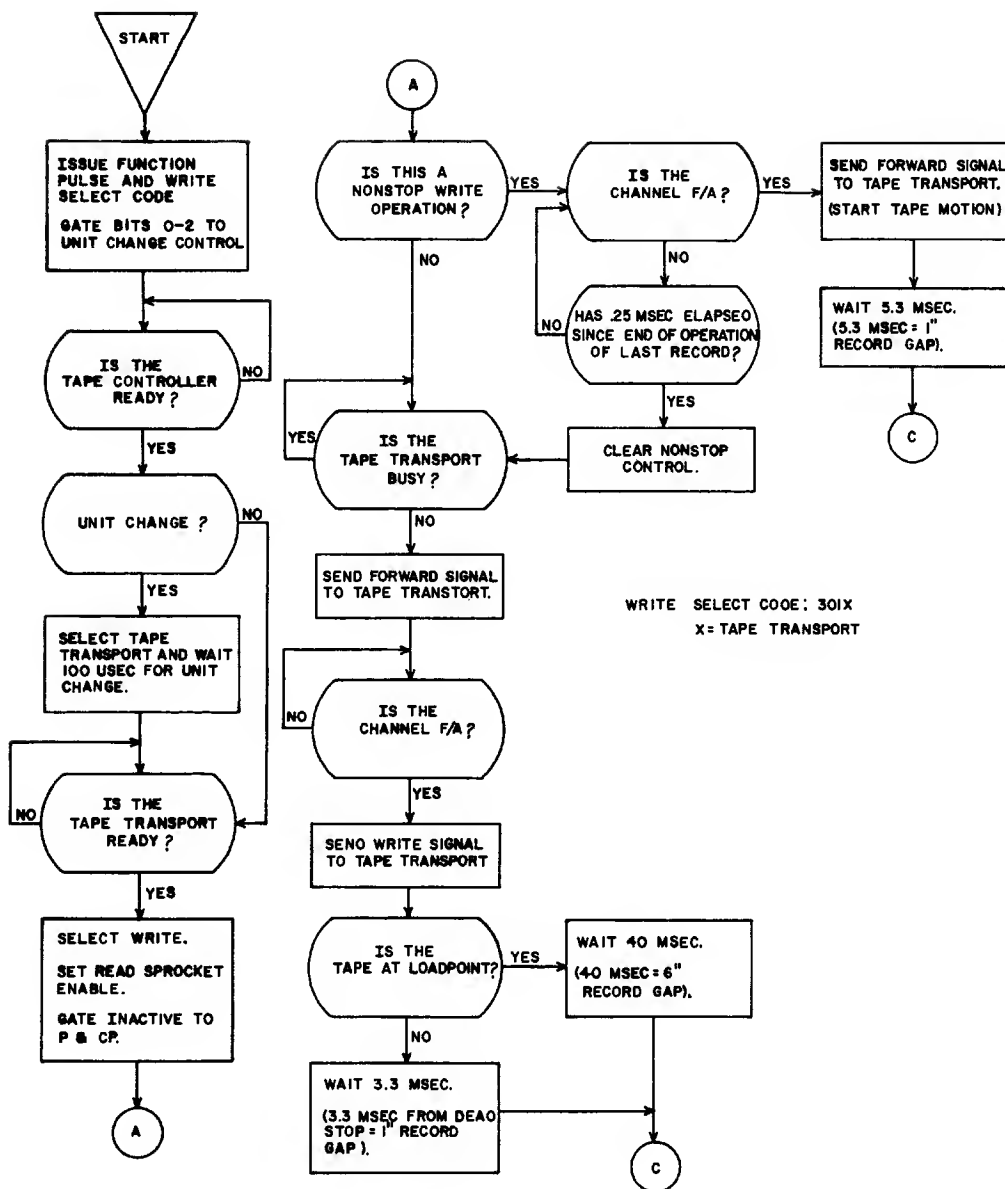




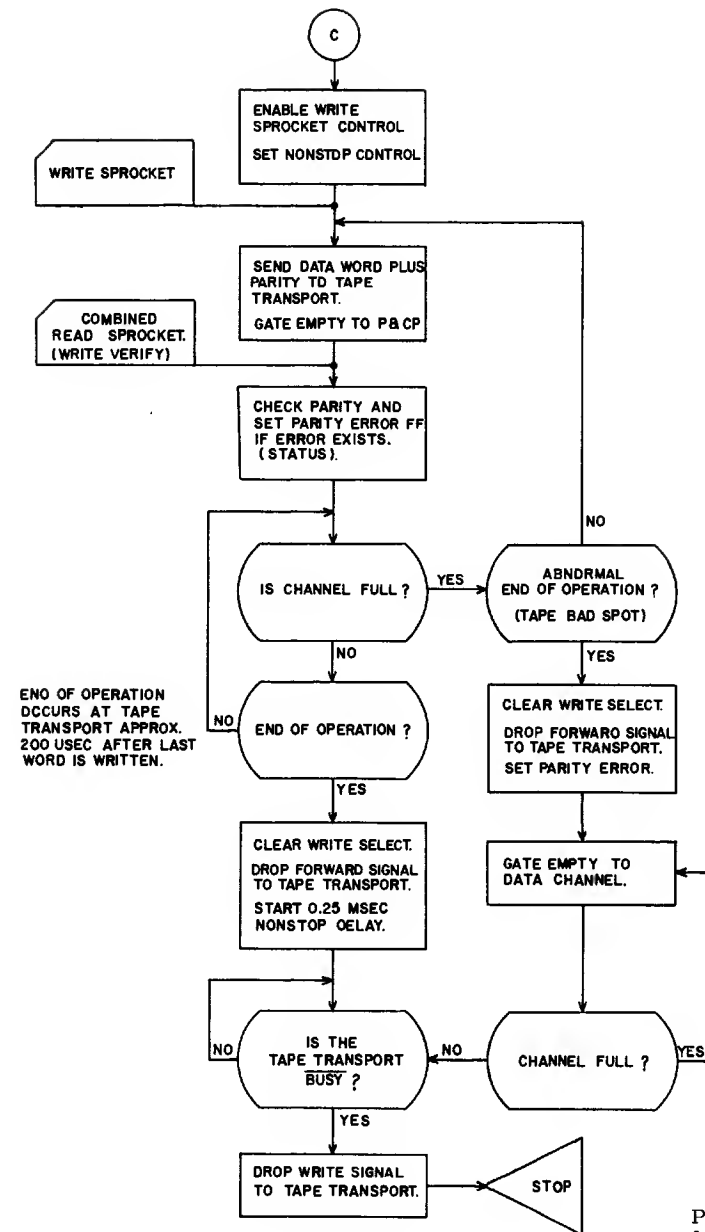
CONTROL DATA
CORPORATION
COMPUTER DIVISION

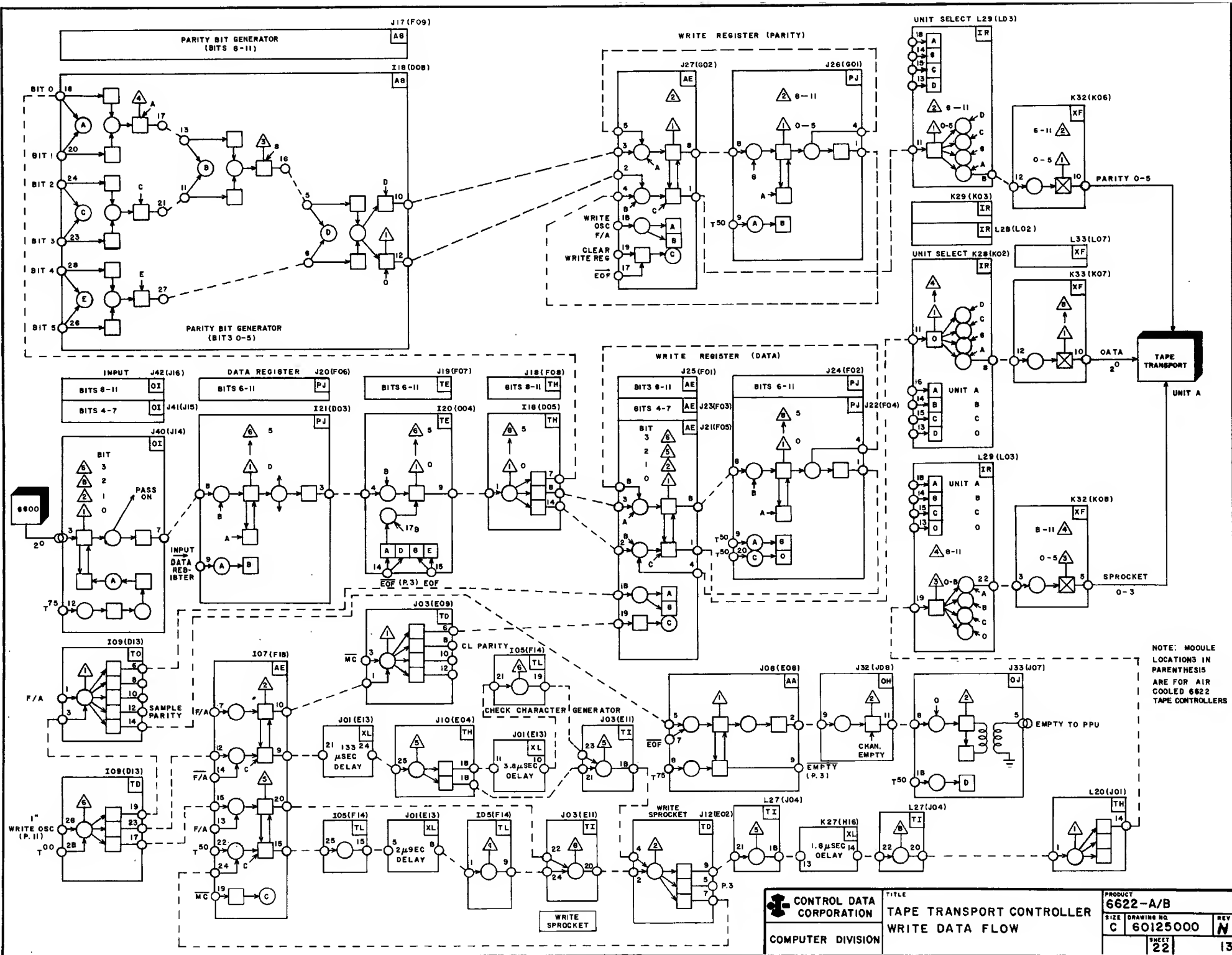
TITLE
TAPE TRANSPORT CONTROLLER
WRITE OSCILLATOR

PRODUCT
6622-A/B
SIZE
C 60125000
SHEET
21
REV
N
11



FLOW CHART
TAPE WRITE OPERATION



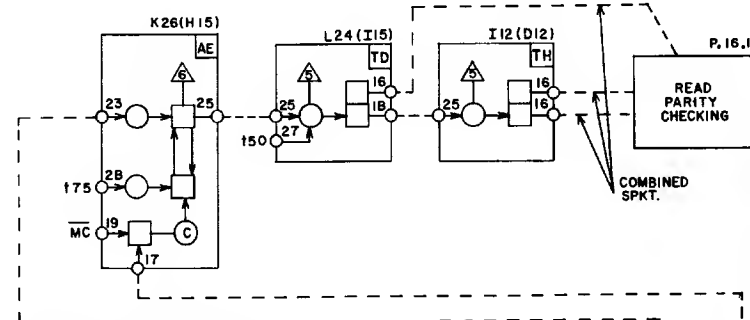
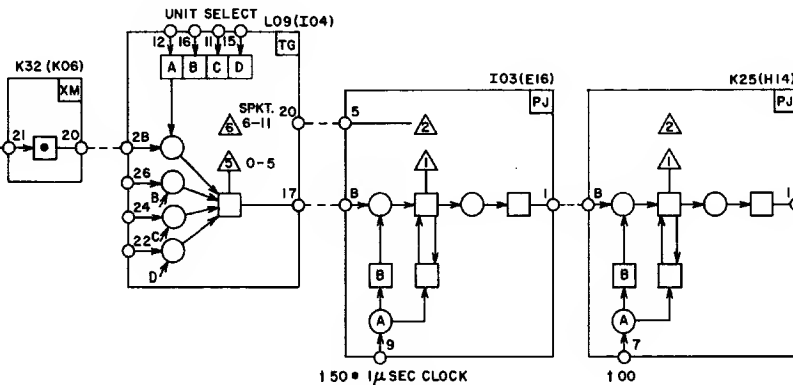


CONTROL DATA
CORPORATION
COMPUTER DIVISION

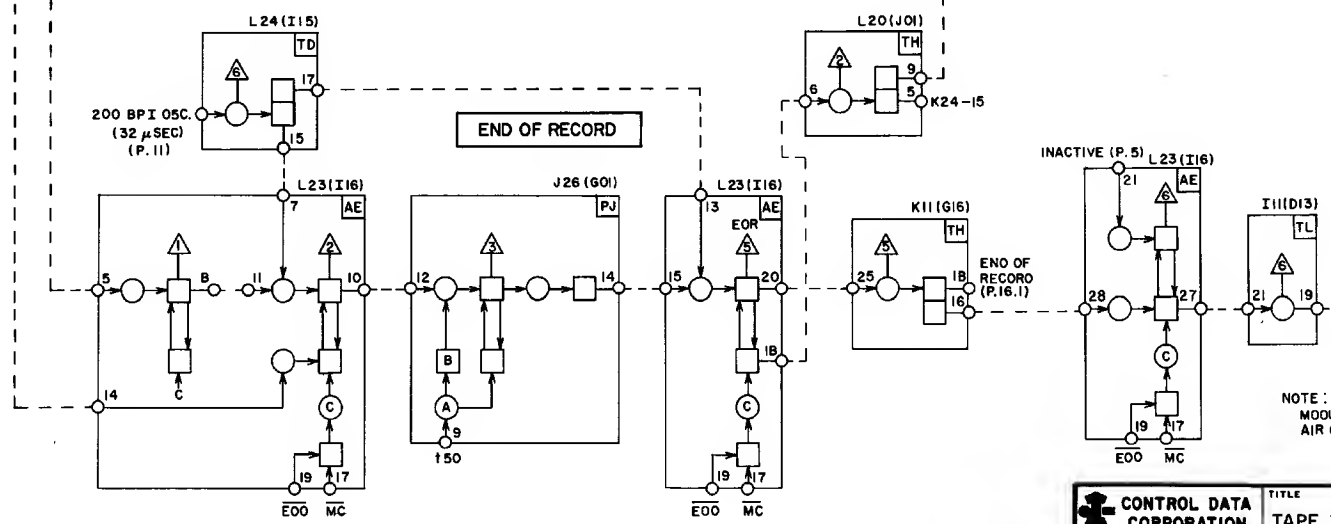
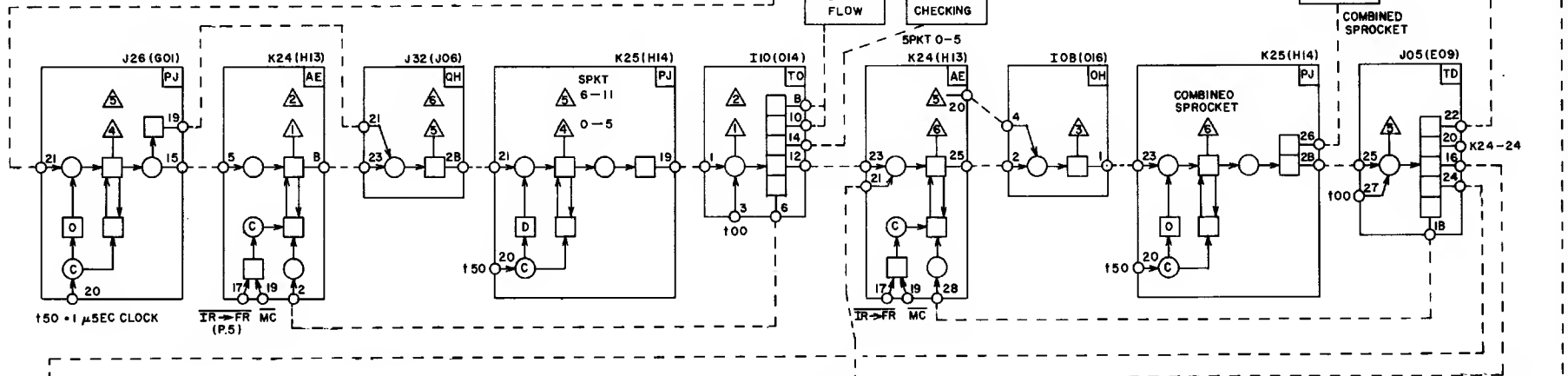
TITLE
TAPE TRANSPORT CONTROLLER
WRITE DATA FLOW

PRODUCT
6622-A/B
SIZE
C
DRAWING NO.
60125000
REV
N
SHEET
22
13

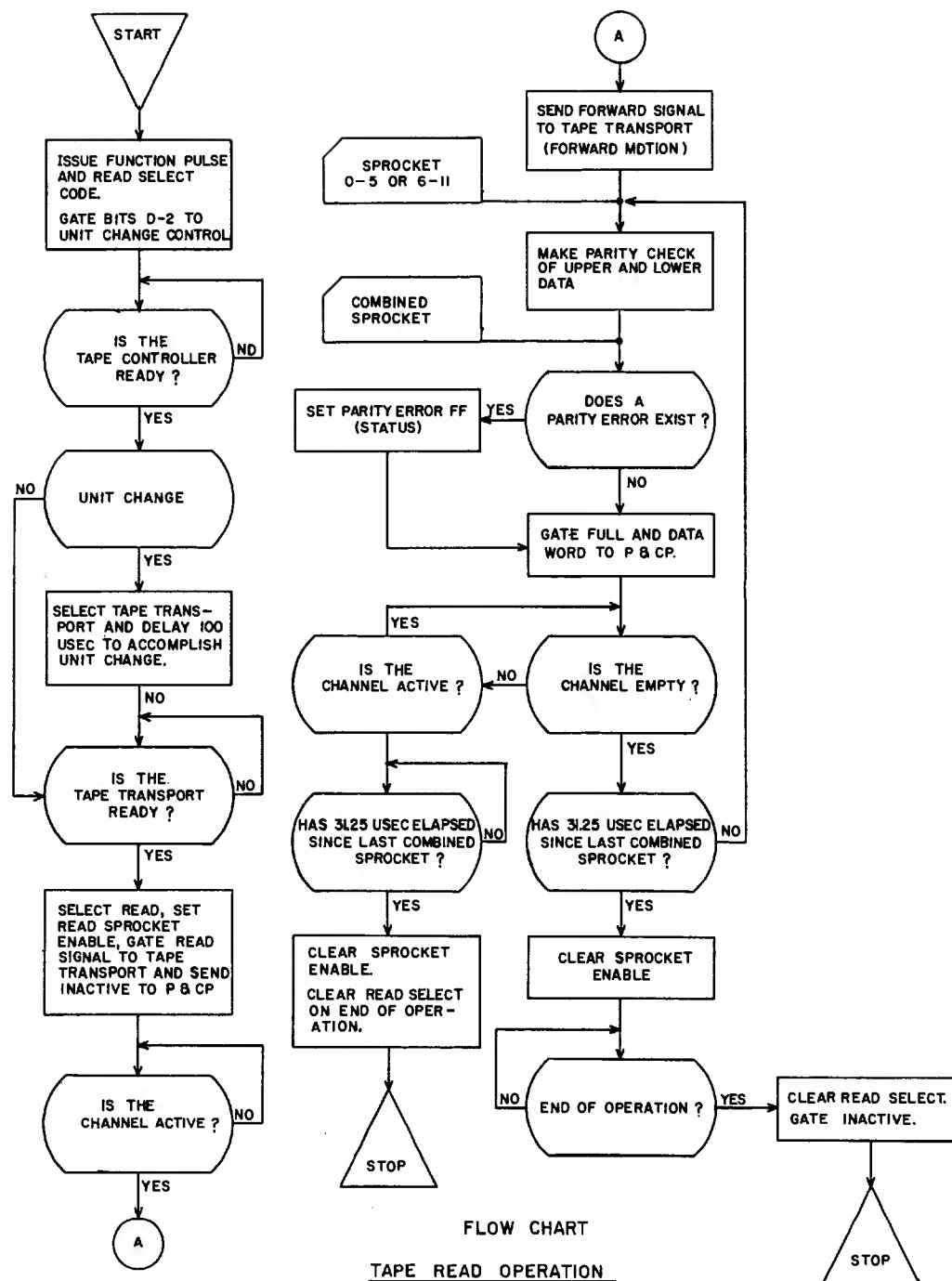
UNIT A
TAPE TRANSPORT



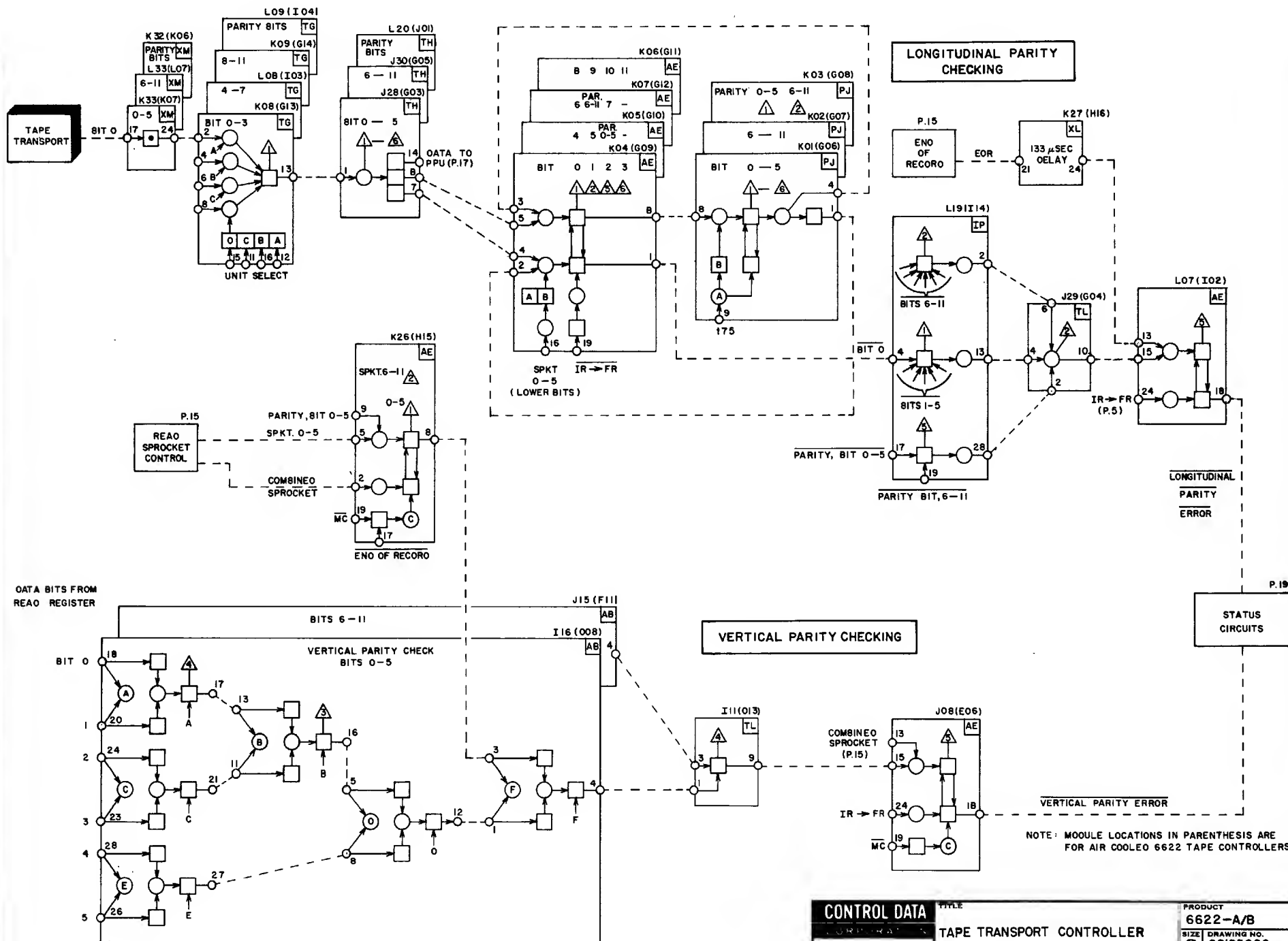
READ SPROCKET CONTROL

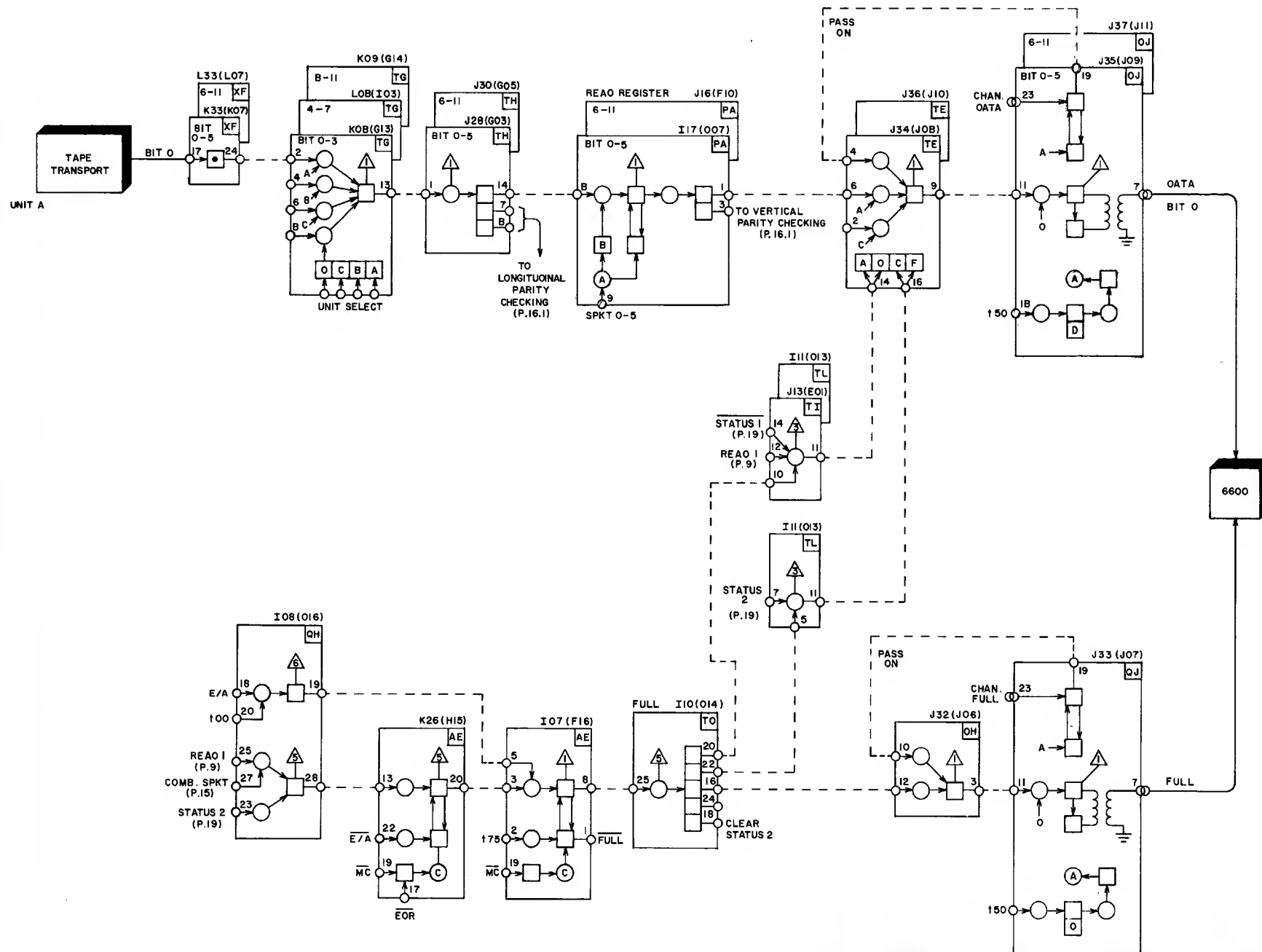


NOTE:
MODULE LOCATIONS IN PARENTHESIS ARE FOR
AIR COOLED 6622 TAPE CONTROLLERS.



FLOW CHART
TAPE READ OPERATION





NOTE:
MODULE LOCATIONS IN PARENTHESIS ARE
FOR AIR COOLEO 6622 TAPE CONTROLLERS.

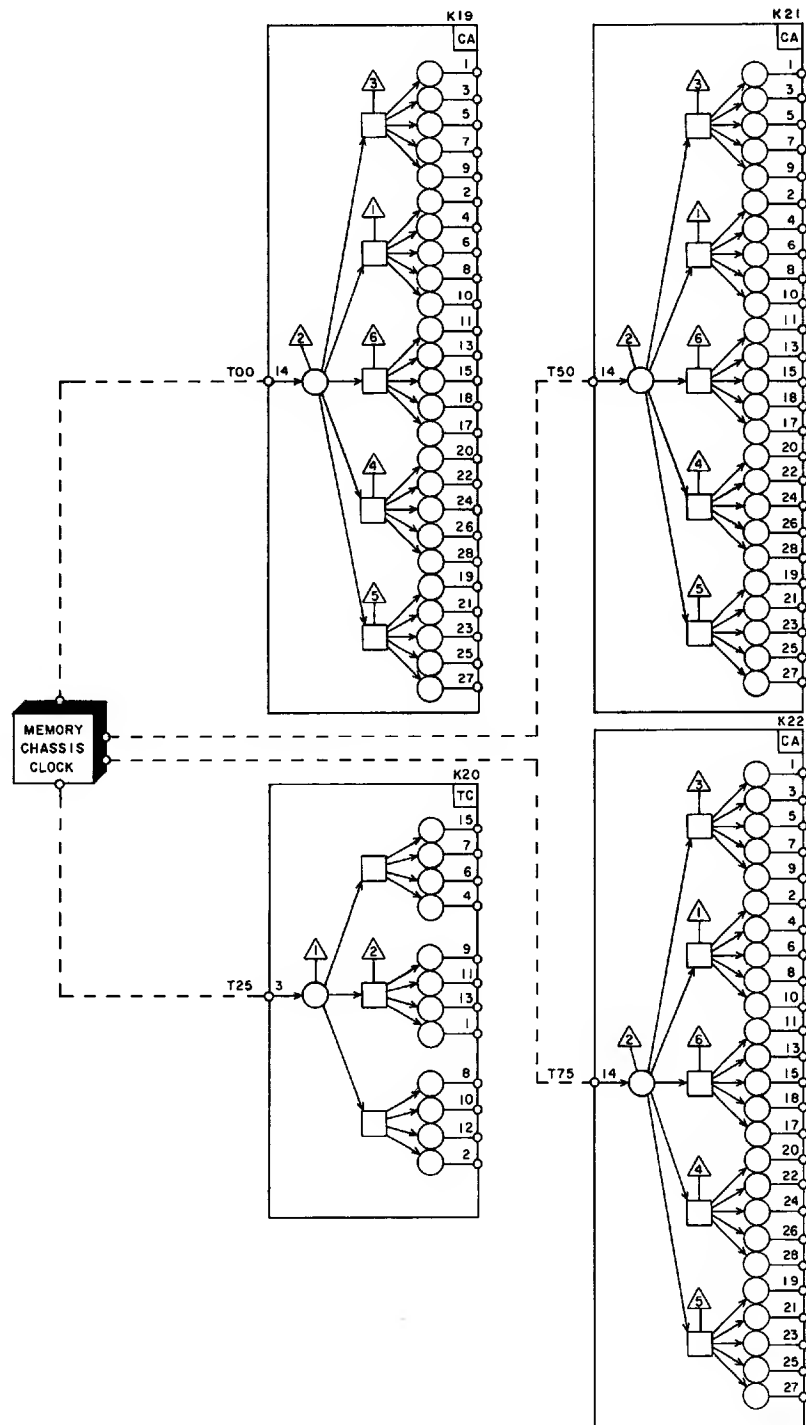
CONTROL DATA CORPORATION
COMPUTER DIVISION

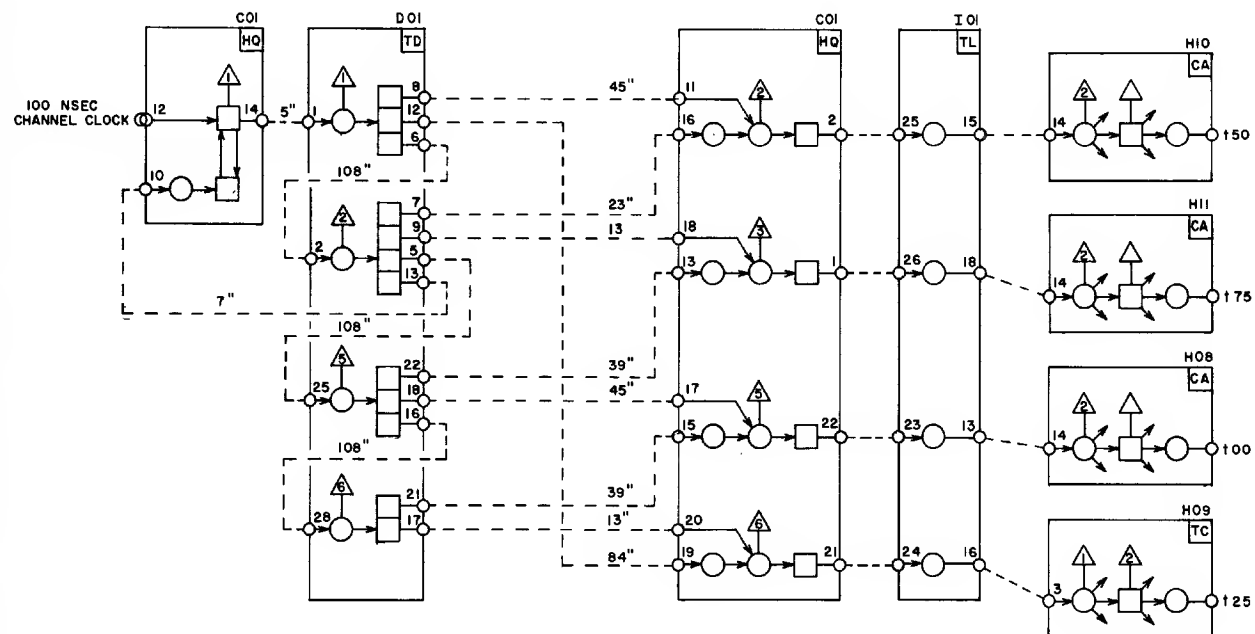
TITLE
TAPE TRANSPORT CONTROLLER
READ DATA FLOW

PRODUCT
6622-A/B
SIZE DRAWING NO.
C 60125000
REV
24 17

1. 40 MS DELAY ALLOWS 6" GAP FROM LOAD POINT TO FIRST WRITTEN CHARACTER.
2. 33 MS DELAY ALLOWS TAPE TO REACH OPERATING SPEED BEFORE WRITE IS ENABLED.
3. 5.3 MS DELAY INSERTS RECORD GAP DURING NONSTOP WRITE. K14 (HO3)







SEE PAGE 23 FOR DETAIL
ON THESE FANOUTS.

6681 DATA CHANNEL CONVERTER

*as to convert from 6000
language to 3000*

CONTENTS

Page	Title
ii	Description and Mode of Operation
1	Block Diagram
2	Module Index and Card Placement
3	Data Flow
5	Mode Selection and Status Review
7	External Equipment Commands
9	Function, Connect and Reply
11	Clock

The 6681 Data Channel Converter allows any 6000 Series Data Channel to communicate with any 3000 Series peripheral equipment.

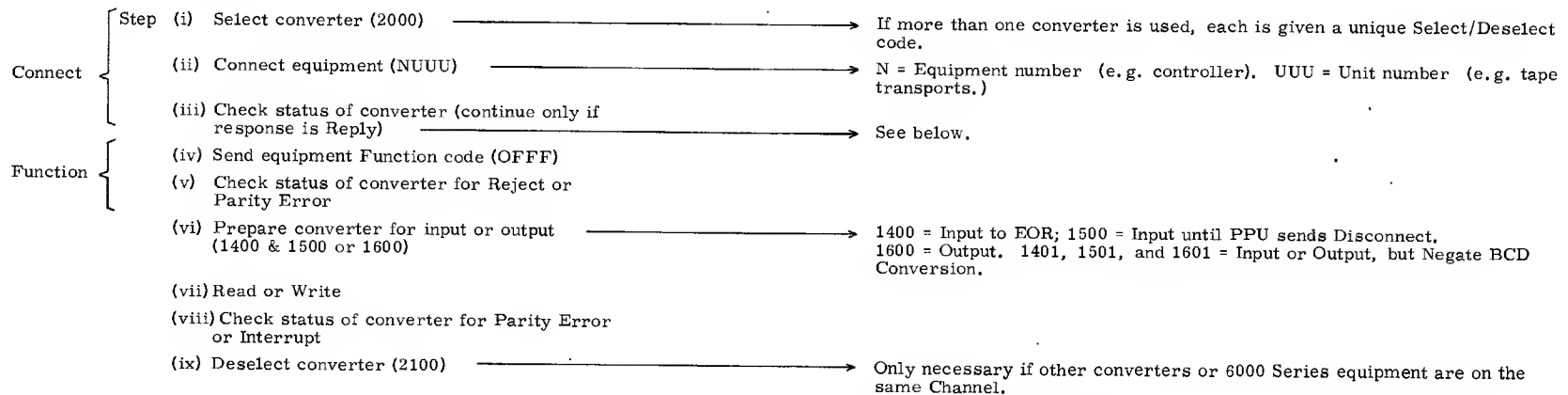
SYSTEM RESTRICTIONS

- (i) While as many as eight converters may be used on a data channel, they must precede any other 6000 Series equipment. This avoids instruction conflicts since a selected converter does not relay information to the other equipment on the channel.
- (ii) The converter must be deselected before other equipments on the channel can be used.
- (iii) Deselecting the converter does not disconnect the equipment.

SEQUENCE OF OPERATION

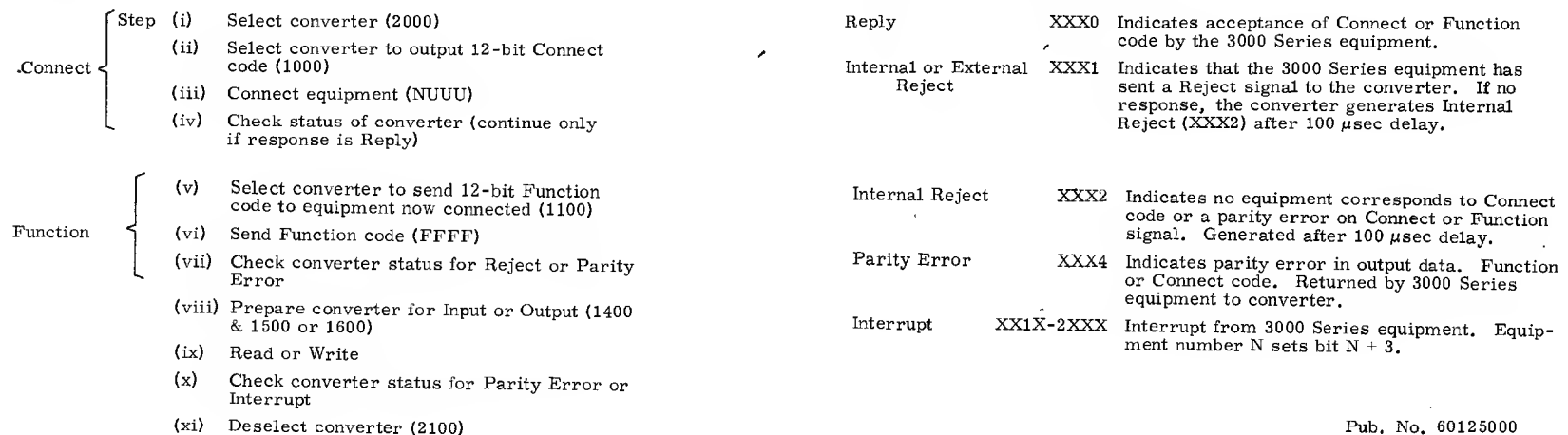
Note that normal operation is with BCD conversion suppressed. Two modes of operation are available:

MODE I This mode reduces programming steps but is limited to: (i) equipments numbered 4XXX-7XXX, and (ii) 3000 Series function codes which have zeros in the upper three bits.



MODE II

CONVERTER STATUS RESPONSES



6681 MODULE INDEX & CARD PLACEMENT

Each module is shown by location and gives the card type and the drawing(s) on which it occurs.

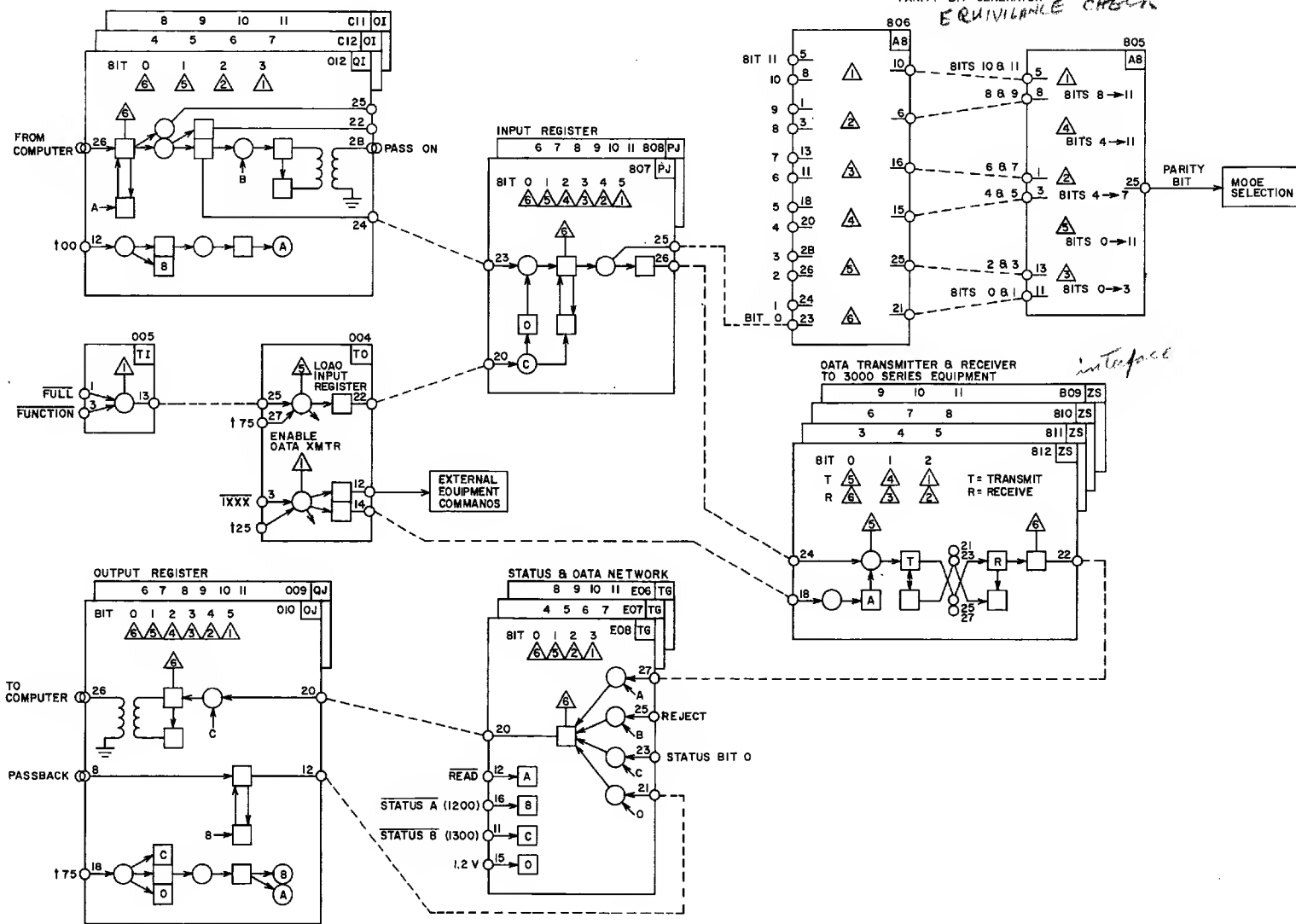
Example: At A6 is a ZR module which is shown on page 5.

	1	2	3	4	5	6	7	8	9	10	11	12
A			TI p.7	ZR p.5	ZR p.5	ZR p.5	ZR p.5	ZR p.5	ZR p.5	ZT p.7, 9	ZT p.7	ZT p.5, 7
B			TL p.5, 7,9	ZG p.7	AB p.3	AB p.3	PJ p.3	PJ p.3	ZS p.3	ZS p.3	ZS p.3	ZS p.3
C			ZF p.5, 7	TH p.5, 7,9	ZD p.5, 7,	IV	TH p.5	CB p.11	QI p.5	QI p.5	QI p.3	QI p.3
D			ZB p.7, 9	TD p.3, 7	TT p.3, 5,7	IV	IV	TC p.11	QJ p.3	QJ p.3	QJ p.7, 9	QI p.3
E		TD p.7	XL p.7, 9	ZC p.7, 9	ZE p.5, 7,9	TG p.3	TG p.3	TG p.3	ZA p.5, 7,9	QH p.11	TD p.11	HQ p.11

NOTE: For information on 6681 cabinets see Control Data Peripheral Controller Cabinets, Pub. No. 60097300.

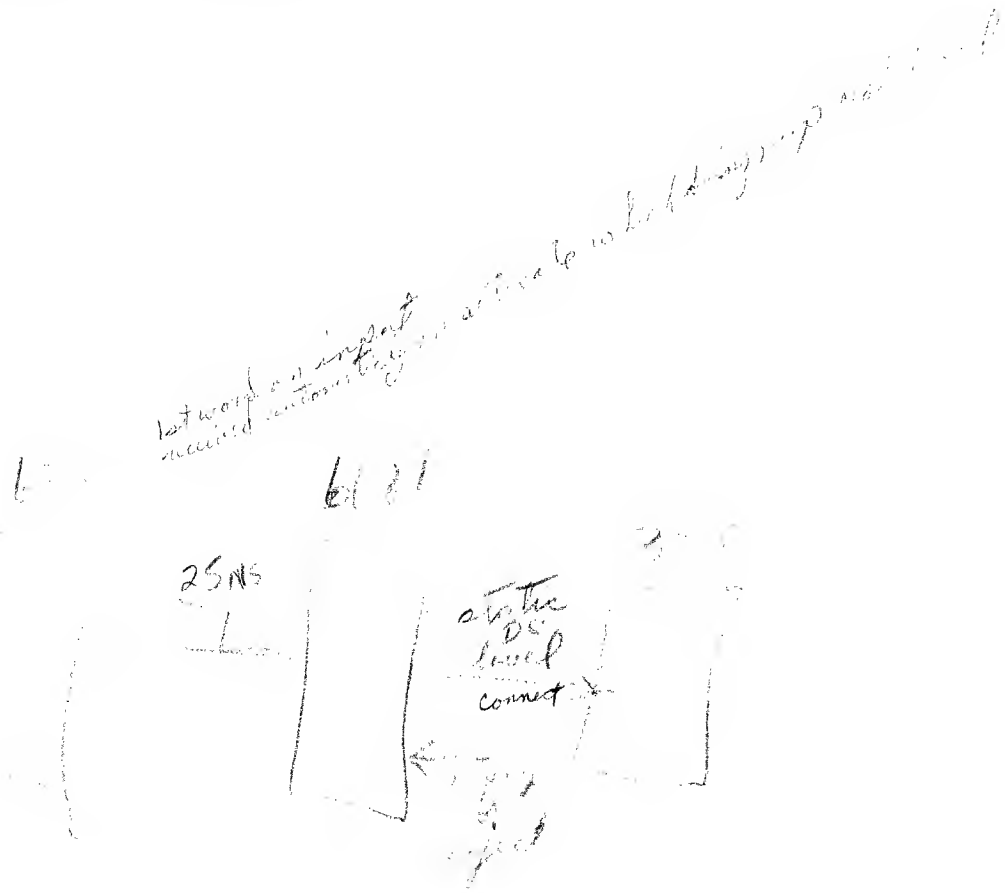
Pub. No. 60125000

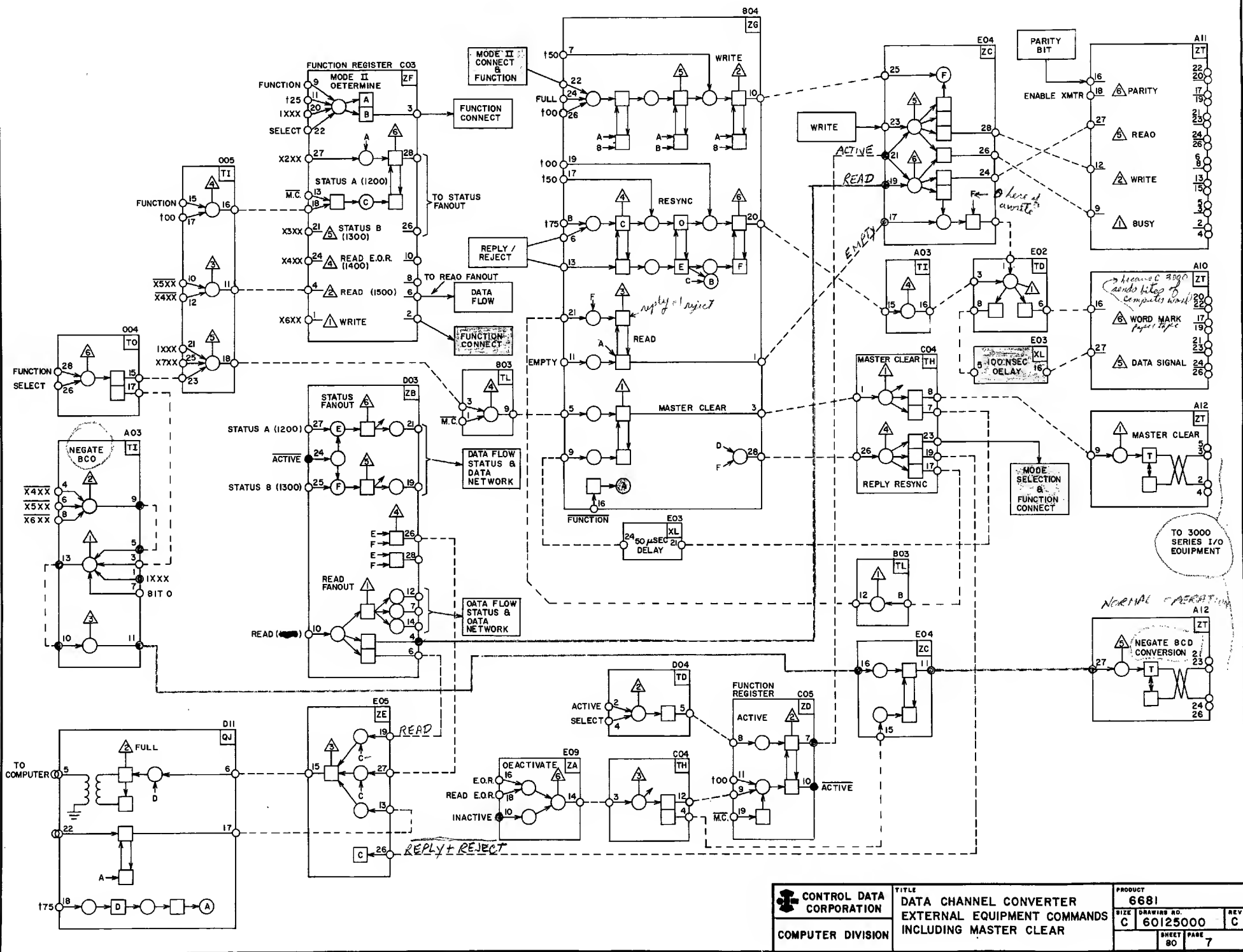
6681 Rev. C 2



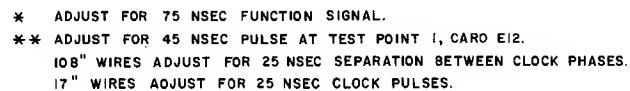
empty from 6600 to 6681 causes 6681 to send a data level to 3000 which will send back reply which causes the 6681 to send full to 6600

full from 6600 causes 6681 to send data to 3000 which send reply to 6681 as an empty in turn sends an empty to 6600









6682 SATELLITE COUPLER

CONTENTS

Page	Title
ii	Description and Mode of Operation
1	Block Diagram
2	Module Index and Card Placement
3	Part 1
5	Part 2
7	Part 3
9	Clock

DESCRIPTION AND MODE OF OPERATION

6682 SATELLITE COUPLER

SEQUENCE OF OPERATION LOCAL COMPUTER OUTPUT

2A TO OUTPUT

- If (i) go to 1
- If (iii) go to 15
- If (ii) or (iv) go to 3

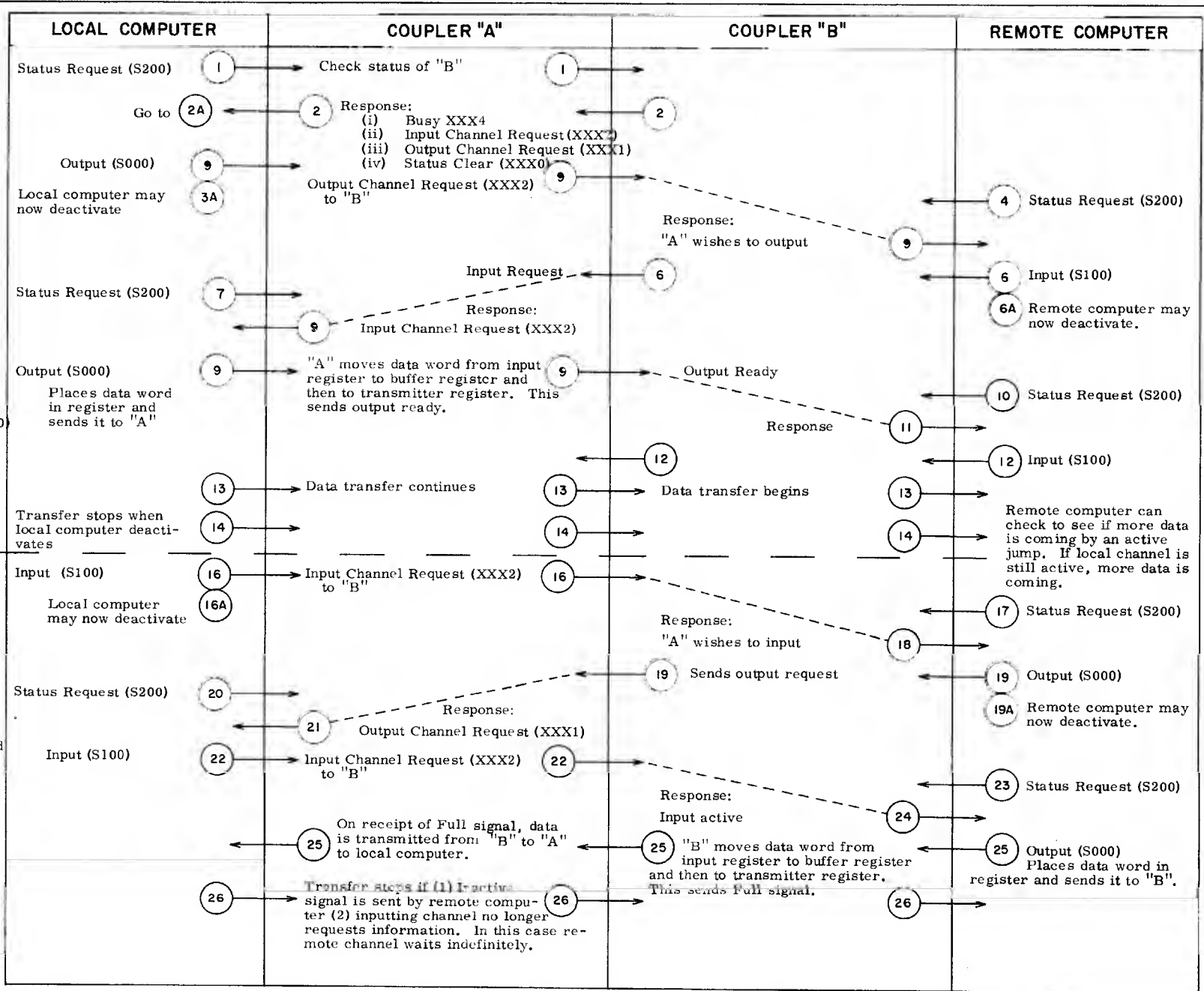
2A TO INPUT

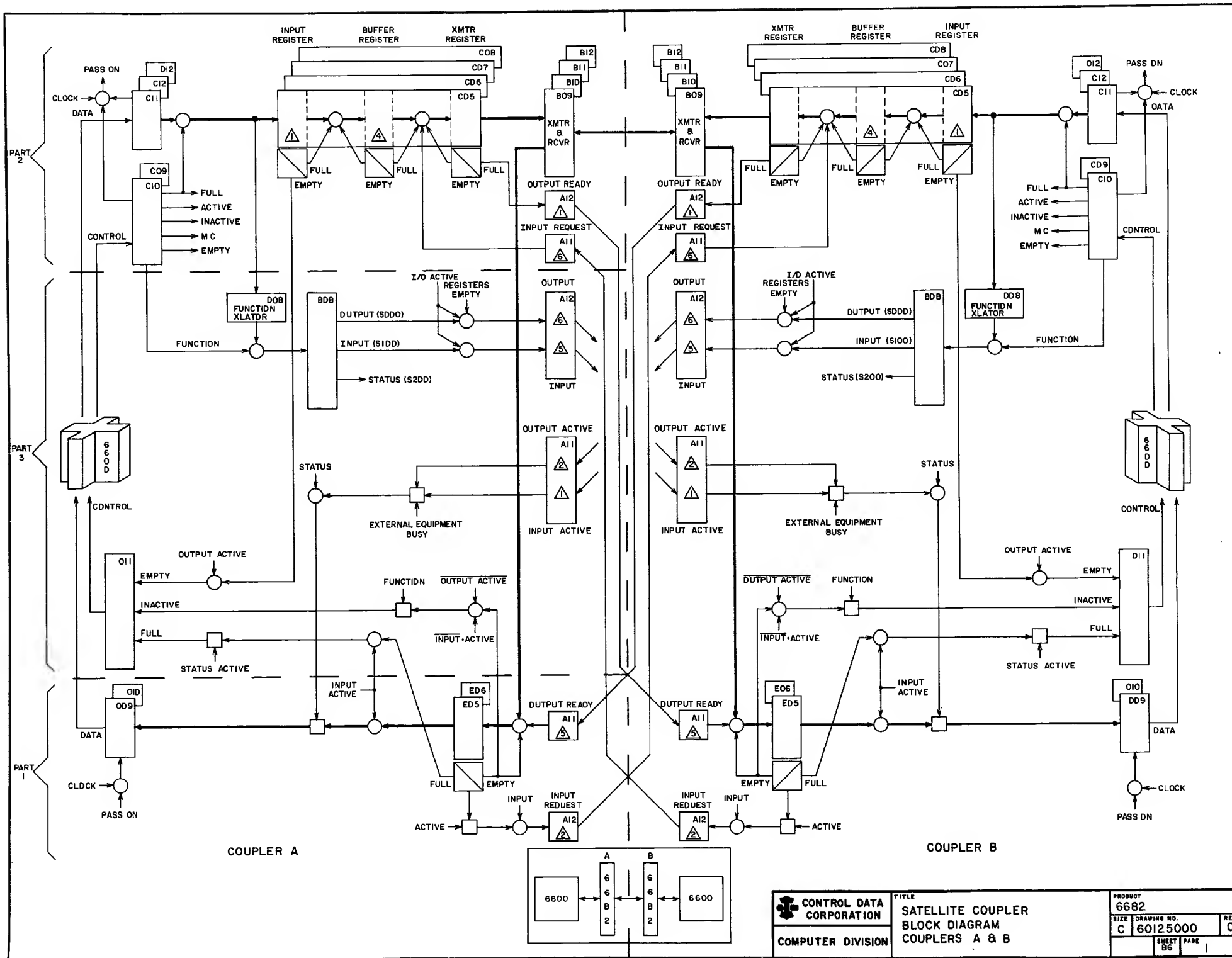
- If (i) go to 1
- If (ii) go to 27
- If (iii) or (iv) go to 16

15 Indicates remote computer wishes to output. If local computer sends Output (S000) then conflict will result. Local computer should respond with Input (S100) and initiate sequence shown, but in reverse.

LOCAL COMPUTER INPUT

27 Indicates remote computer wishes to input. If local computer sends Input (S100) then conflict will result. Local computer should respond with Output (S000) and initiate sequence shown but in reverse.





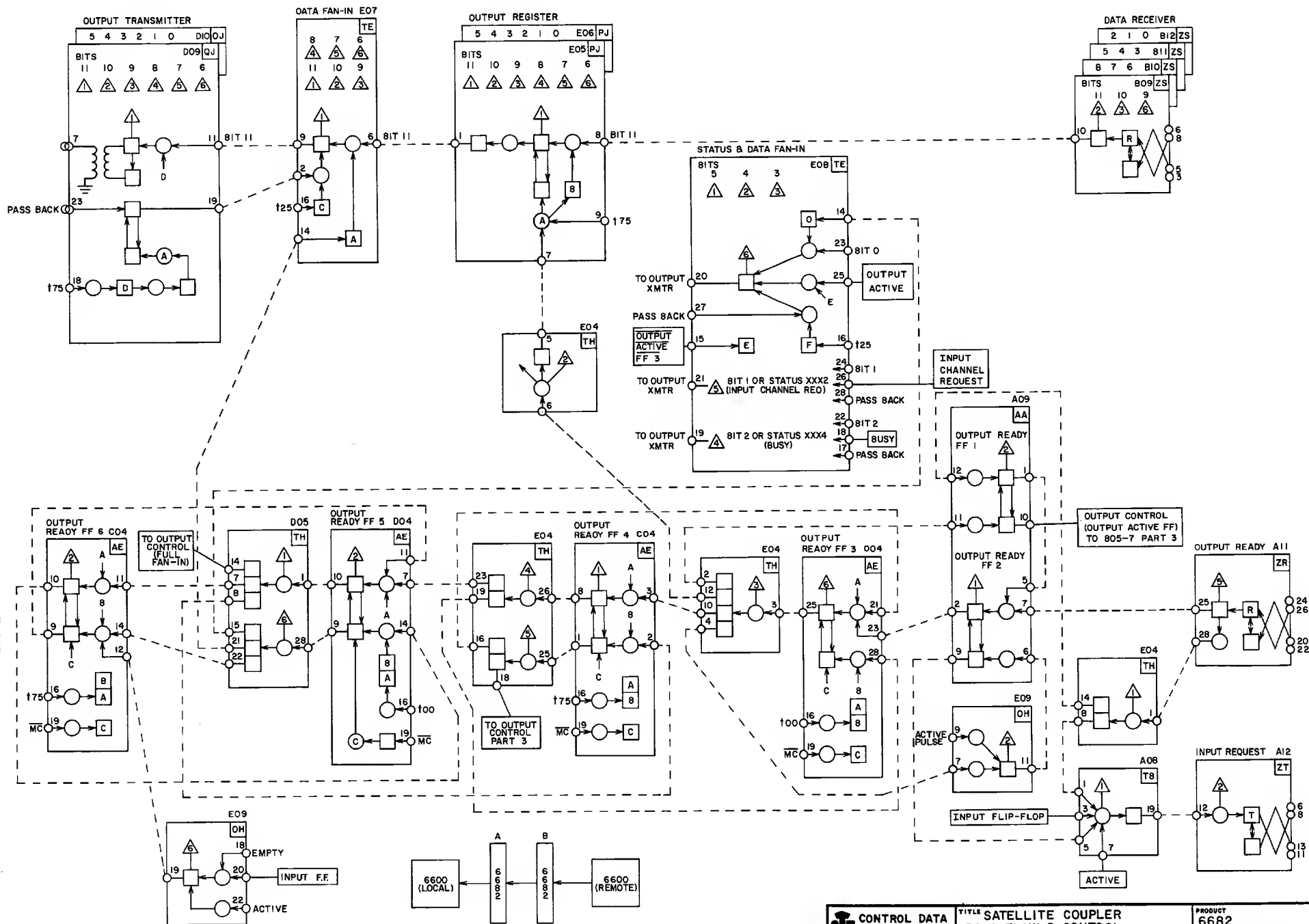
6682 MODULE INDEX & CARD PLACEMENT

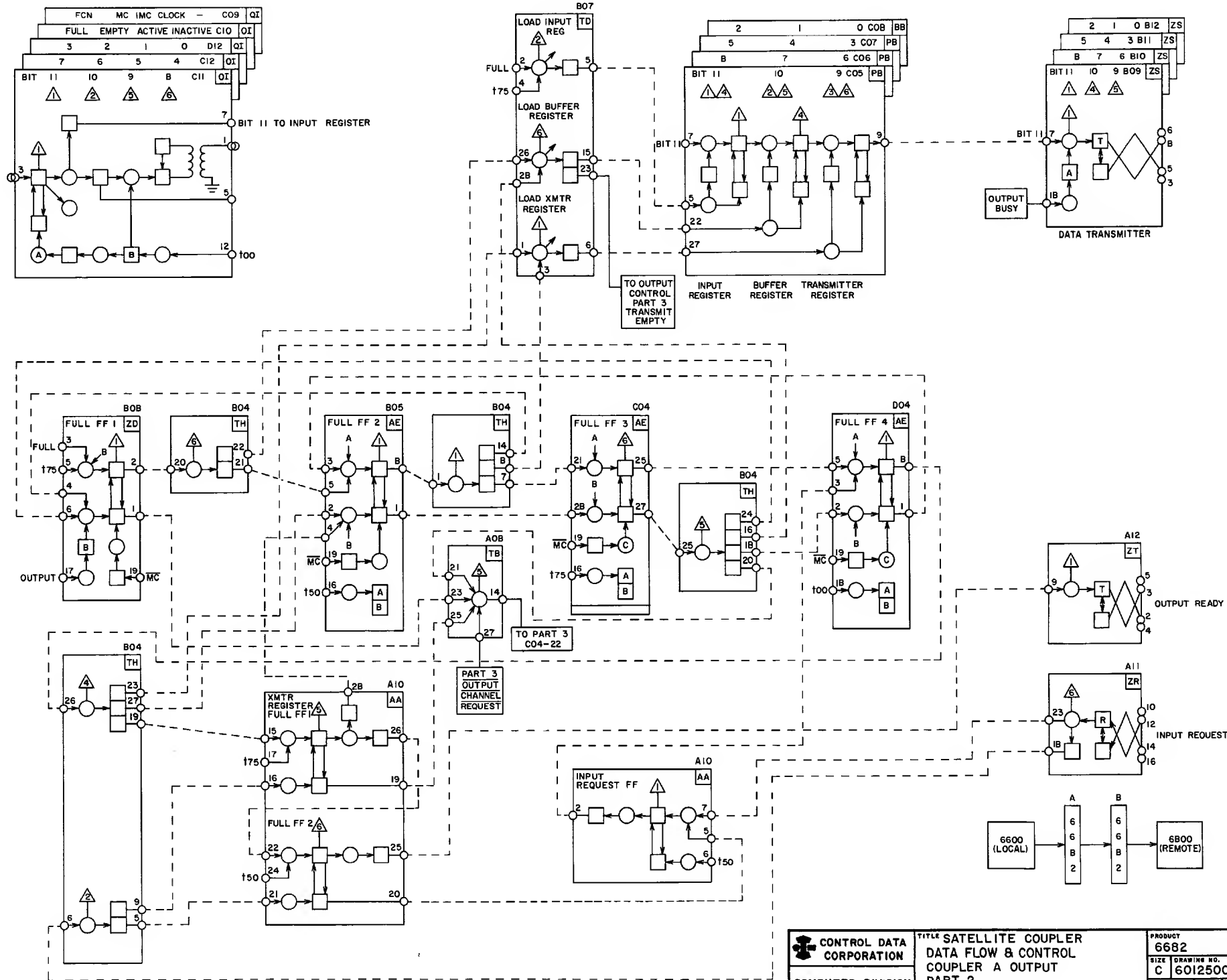
Each module is shown by location and gives the card type and the drawing(s) on which it occurs.

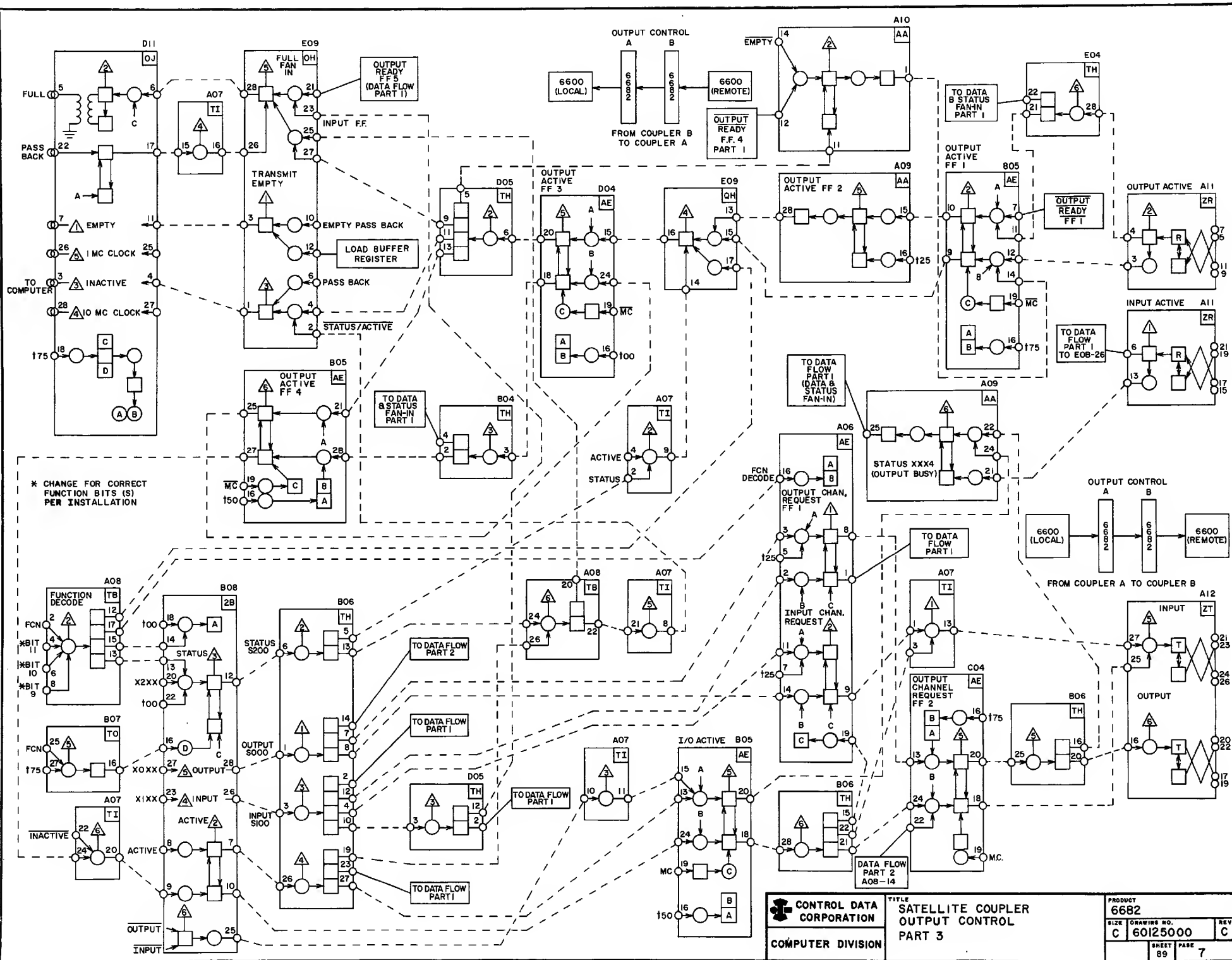
Example: At A6 is an AE module which is shown on page 7.

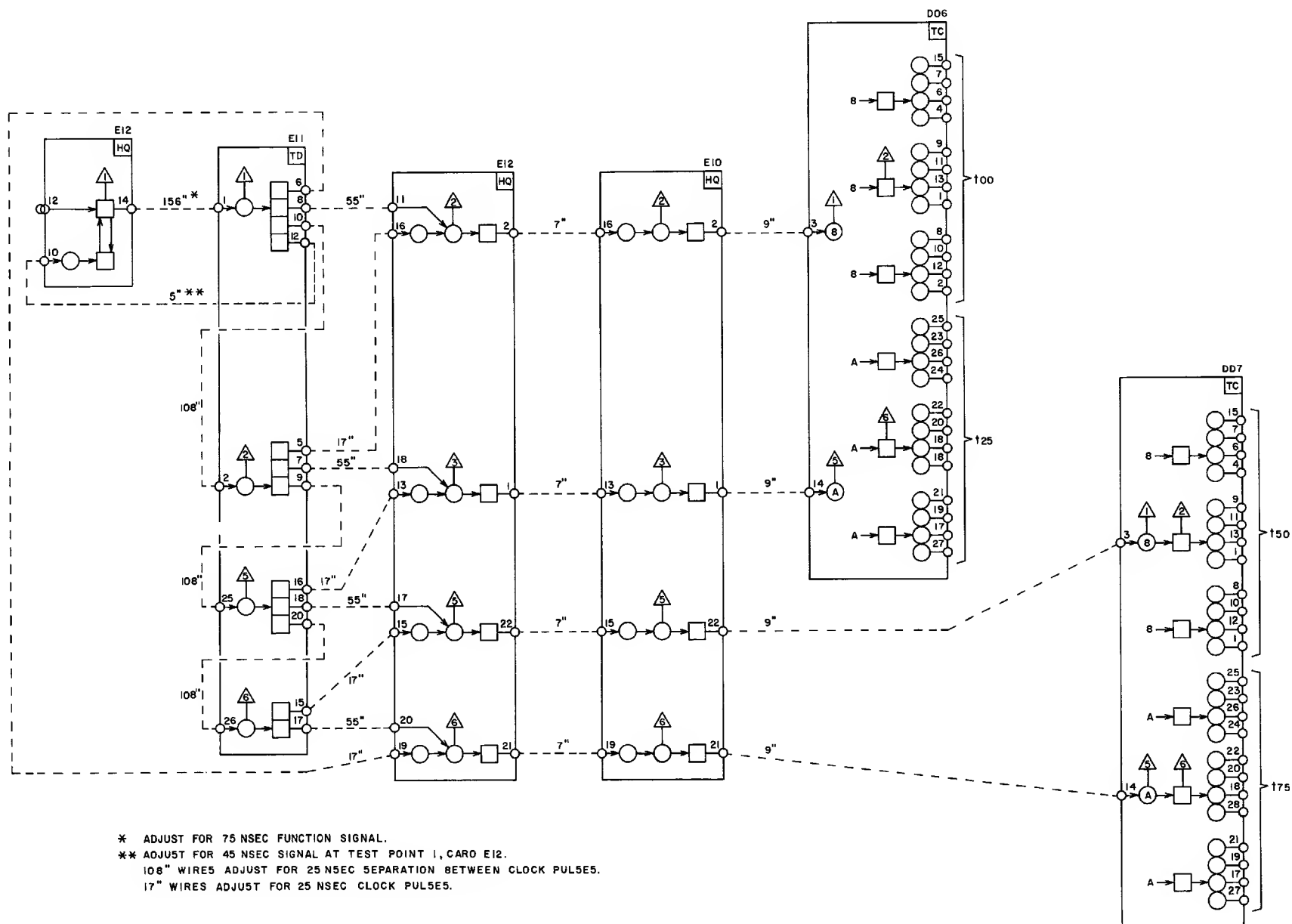
	1	2	3	4	5	6	7	8	9	10	11	12
A						AE p.7	TI p.7	TB p.3, 5,7	AA p.3, 7	AA p.5, 7	ZR p.3, 5,7	ZT p.3, 5,7
B				TH p.5, 7	AE p.5, 7	TH p.7	TD p.5, 7	ZD p.5, 7	ZS p.3, 5	ZS p.3, 5	ZS p.3, 5	ZS p.3, 5
C				AE p.3, 5,7	PB p.5	PB p.5	PB p.5	PB p.5	QI p.5	QI p.5	QI p.5	QI p.5
D				AE p.3, 5	TH p.7	TC p.9	TC p.9	IV ---	QJ p.3	QJ p.3	QJ p.7	QI p.5
E				TH p.3, 7	PJ p.3	PJ p.3	TE p.3	TE p.3	QH p.3, 7	HQ p.9	TO p.9	HQ p.9

NOTE: For information on 6682 cabinets see Control Data Peripheral Controller Cabinets, Pub. No. 60097300.









S.O. 60022 6000 SERIES DATA CHANNEL CONVERTER (1612 PRINTER)

CONTENTS

Page	Title
ii	1612 Line Printer Controller
1	Function Circuits
2	Basic Principles of Operation
3	Data Control
4	Resynchronization
5	Data Flow
6	1612 Printer Characteristics
7	Clock

1612 LINE PRINTER CONTROLLER

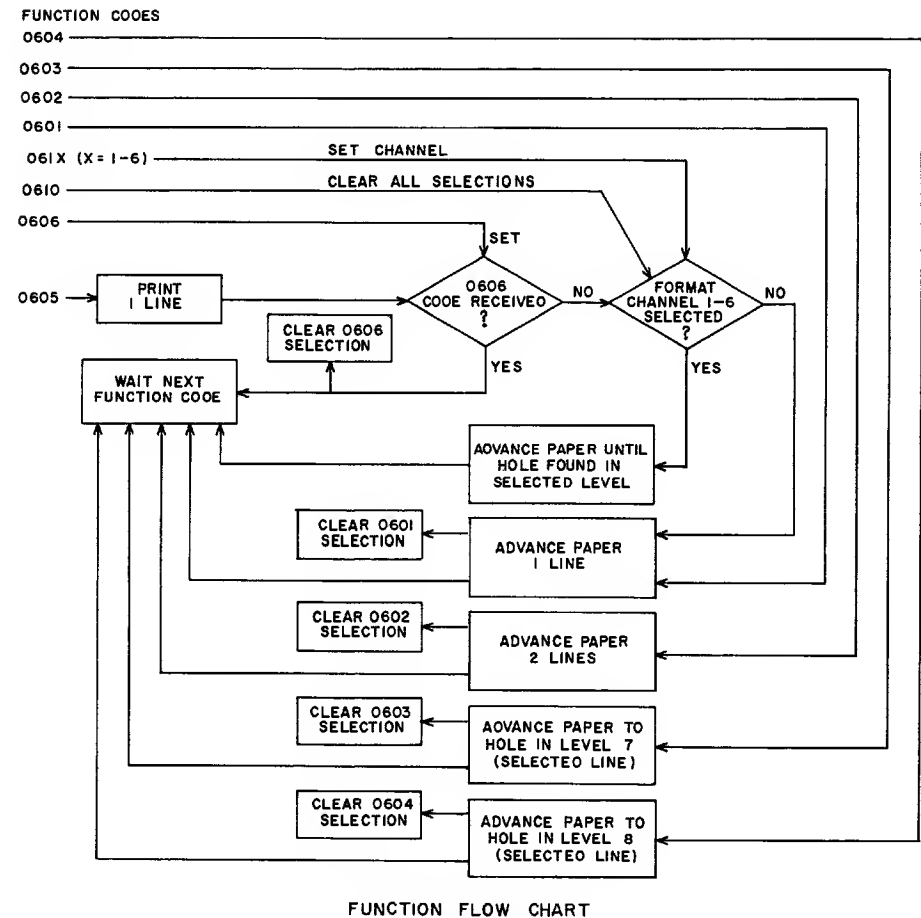
The CONTROL DATA 6600 Computer System operates the 1612 Line Printer via a peripheral controller which simulates a 160 computer I/O interface. The peripheral controller is discussed below and a brief description of the 1612 Line Printer may be found on page 6.

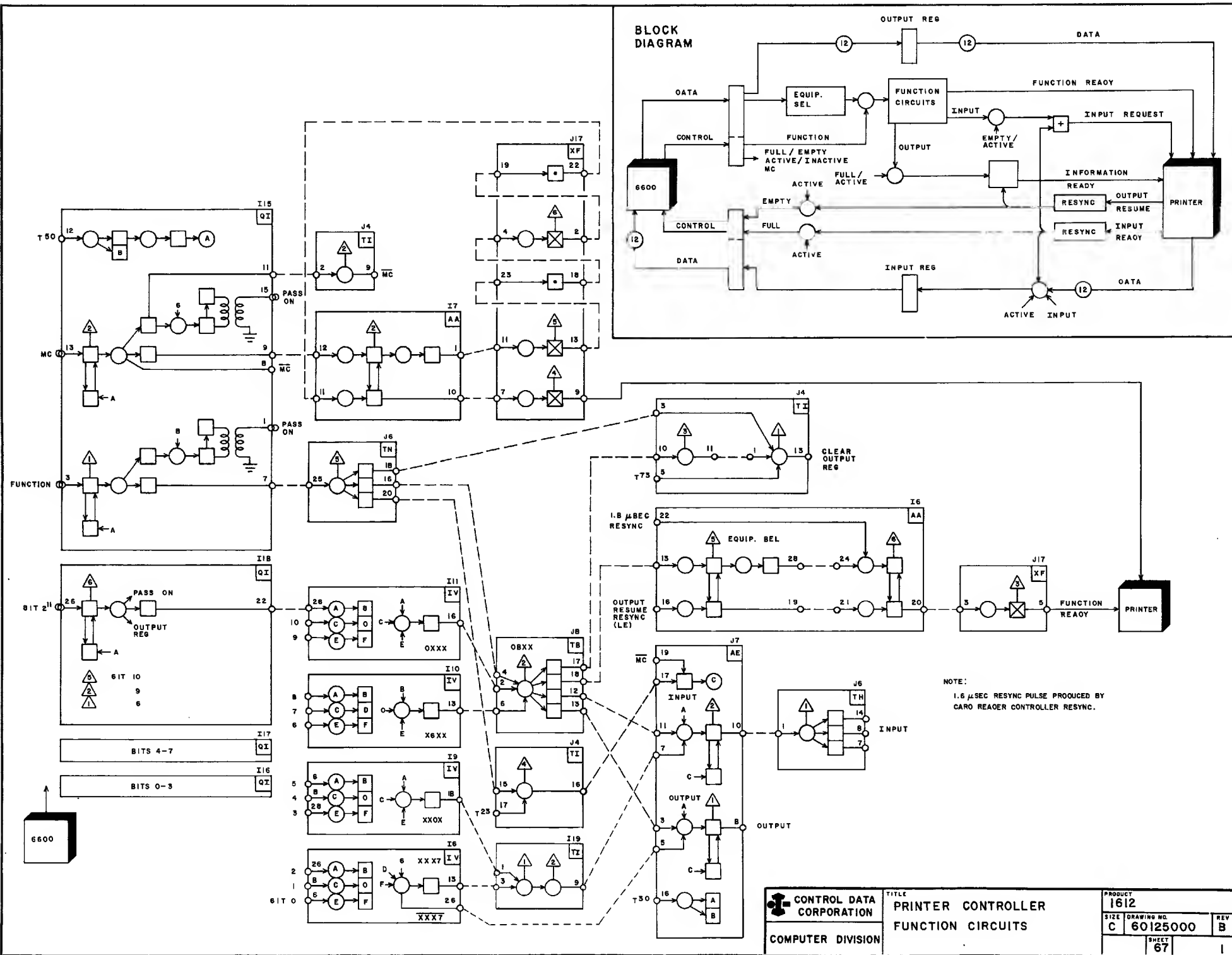
1612 SELECT INSTRUCTIONS

- 0600 Select Printer for Output operation.
- 0605 Print. This must follow each output buffer operation to initiate the print/advance cycle.
- 0606 Suppress paper advance after next print. This function eliminates the automatic paper advance at the end of a print cycle. This function is cleared after one line has been printed.
- 0601 Advance paper one line. The advance is executed on receipt of the function, and the selection is cleared when the spacing operation terminates.
- 0602 Advance paper two lines. The advance is executed on receipt of the function, and the selection is cleared when the spacing operation terminates.
- 0603 Advance to selected line. The advance is executed on receipt of the function, and the selection clears when the spacing operation terminates. Channel 7 of the format tape is selected, and a hole in the seventh level of the tape terminates the advance.
- 0604 Advance to top of form. The advance is executed on receipt of the function, and the selection clears when the spacing operation terminates. Channel 8 of the format tape is selected and a hole in the eighth level of the tape terminates the advance. Level 8 of the format tape should have one hole punched, and paper is aligned with this when loaded in the printer.
- 0607 Status request. Select the printer for an input operation. Bit 2¹¹ of the input word signifies read/not ready. All other bits are zero. This is the only input word the printer can generate.

Status Response 4000 - Ready
 0000 - Not Ready

- 061X Select format channel, where X = 1 through 6. Move paper after a print cycle until a hole is found in the selected channel. Selection remains until cleared by an 0610 function or a master clear.
- 0610 Clear all format channel selections 1 through 6.





BASIC PRINCIPLES OF OPERATION

Peripheral and Control Processors communicate with peripheral controllers via a data channel and co-axial signal lines. The controller accepts data and control bits from the data channel register, and one minor cycle later relays these bits to the next controller on that channel. It must also accept data and control bits from that controller, and one minor cycle later, relay these back to the data channel register. The 1612 controller communicates with the 1612 via two twisted pair cables.

DESELECT. The 1612 controller is deselected when a function pulse is sent with a function word which does not contain a 1612 code. When not selected, the controller acts as a relay only. No commands are gated to, or accepted from, the 1612 printer.

SELECT. Function code bits are taken from the QI modules to IV modules for translation. The Function pulse is taken two inversions away from the QI and combined with the 06XX translation. Since the only input word the 1612 can generate is status, the presence or absence of the Status Request code is used to select Input or Output. Function and Equipment code combine with status/ $\overline{\text{status}}$ to set Input or Output, and Function and Select send the Function Ready signal to the 1612. The Function Ready remains up until the 1612 sends back an Output Resume.

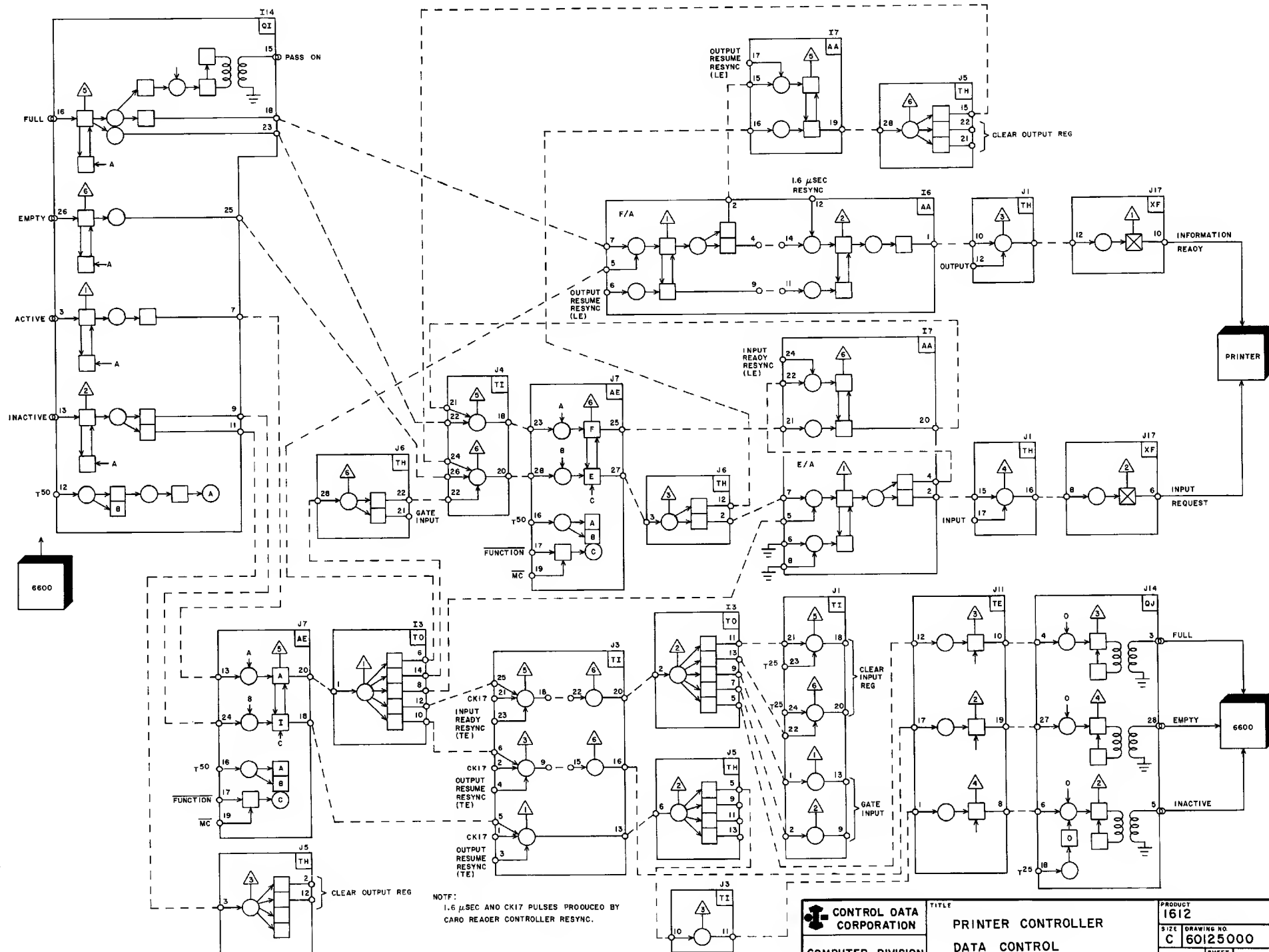
The 12 data bits from the QI modules go to the output register which directly feeds line drivers to the 1612, so that all data from the peripheral processor goes to the 1612. However, the 1612 will accept this data only when accompanied by a Function Ready or an Output Ready command.

INPUT. If, on receipt of a function pulse, the controller translates the 1612 Status Request code, it sets itself for an Input operation. The controller combines Equipment Select and Function to send a Function Ready command to the 1612. The function code is in the output register, and the output register feeds directly to the 1612 data lines. The Function Ready command remains until the 1612 sends an Output Resume to the controller. Output Resume

clears Function Ready, clears the output register, and sends an inactive pulse to the data channel.

To input the status word from the 1612, the controller combines Input selected, channel Active, and channel Empty to send an Input Request command to the printer. The Input Request remains up until the printer sends the 12-bit status word and an Input Ready to the controller. Data from the 1612 goes directly into the input register. Input Ready causes the controller to drop the Input Request, which then causes the 1612 to drop Input Ready. Input selected, channel Active, channel Empty, and the trailing edge of Input Ready gate the 12-bit status word and a Full pulse to the data channel register. The input register is then cleared at time 25. (Status response is the only word the printer may generate.)

OUTPUT. The controller unconditionally sets its output register with all of the output information from the data channel. The output register is fed directly to the 1612 data lines. If, on receipt of a function pulse, the controller translates select bits for the 1612, it sends a Function Ready command to the 1612. If the function code is not a Status Request, the controller sets itself for an output operation. The Function Ready command remains up until the printer sends an Output Resume. This clears the Function Ready command, and sends an Inactive pulse to the data channel. Function Ready dropping causes the 1612 to drop the Output Resume. The controller utilizes Output Selected, channel Full, and channel Active to generate an Output Ready signal for the printer. (Channel Full indicates data on the lines, and all channel data goes directly through the output register to the printer.) The Output Ready drops when the printer sends back an Output Resume, which then causes the printer to drop the Output Resume. Channel Full, channel Active, and Output Resume cause the controller to clear its output register and send an Empty pulse back to the data channel. This sequence continues until the channel goes Inactive.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE
PRINTER CONTROLLER
DATA CONTROL

PRODUCT
1612
SIZE DRAWING NO.
C 60125000
SHEET
68
REV
3

RESYNCHRONIZATION

An asynchronous pulse from an external device is synchronized with the system clock by an XH module. Under static no-signal conditions, the first three flip flops are set. When the input signal goes to the logic "1" condition, it is gated by a clock pulse, a synchronizer pulse from the counter, and another clock pulse. The same gating occurs when the input goes to the "0" state. The last two flip-flops in the chain are statically clear. When the input clears flip-flop C/D, test

point 6 sets. This enables test point 5, and 5 sets when flip-flop C/D has been reset after the input returns to "0". Test point 6 clears with a 75 clock pulse, and cannot reset until the input makes another cycle.

XF MODULE

This module converts the signal levels of 160 equipment line drivers and receivers to the 6600 type logic in the controllers. A logic "0" on the line is -16 to -20 volts, and a logic "1" is ground level on the line. Threshold of the receiver is approximately -8 volts.

1612 PRINTER CHARACTERISTICS

Number of Characters	64 Including Blank
Printing Rate	Standard FORTRAN Set, 1000 lines per minute All Drum Characters, 500 lines per minute
Line Length	120 Columns (Characters)
Line Spacing	6 Lines Per Inch
Character Spacing	10 Characters Per Inch
Vertical Format	Controlled by 8 Level Prepunched tape

LINE PRINT OPERATION

Each output word received by the 1612 contains a 6-bit code in the low-order bits which specifies one of the 64 different characters that may be printed. The 1612 stores each character to be printed in its own core storage unit. The first character received and stored will be printed in column one, the second character received and stored will be printed in column two, etc. The number of output words sent to the printer is the number of characters which will be printed on that line. If a line is to contain only 20 characters, only 20 words are sent to the printer. Any attempt to include more than the maximum of 120 characters in one line will result in a malfunction.

A print operation is initiated by a Print function code 0605. The 1612 reads (and clears) its core memory, and prints that information. At the end of a print operation, the 1612 advances the paper, and is then ready to receive the next line of characters to be printed.

LINE SPACING OPERATIONS

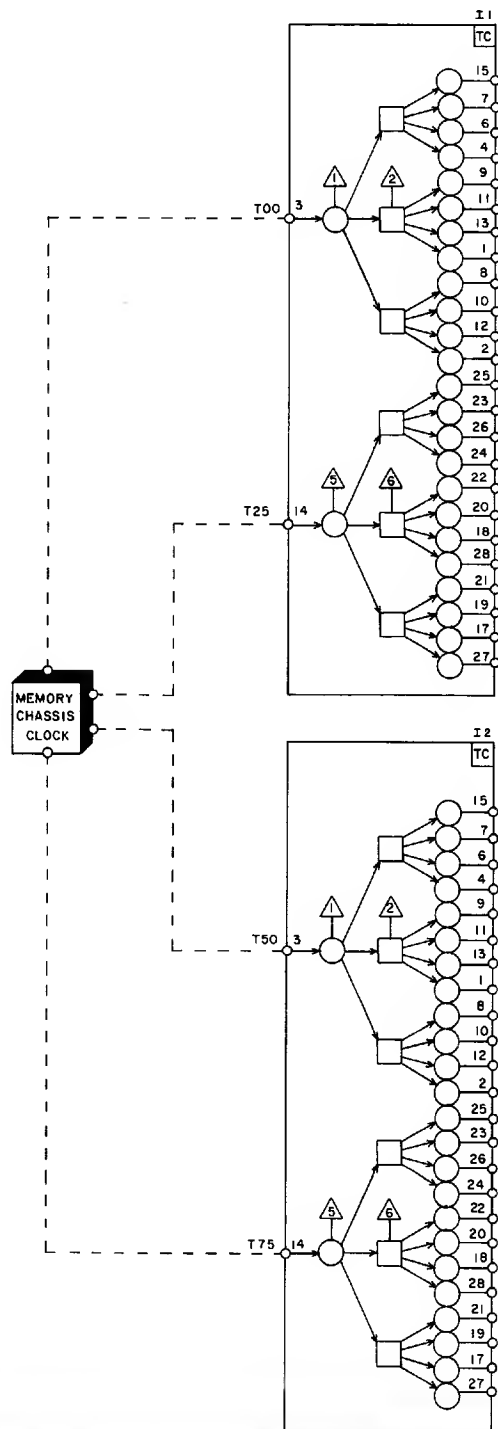
A continuous loop of 8-level punched paper or Mylar tape in the printer controls variable spacing. This tape contains one frame for each line on a page, and is advanced one frame each time the paper advances one line. If a hole is sensed in the selected level or channel, paper motion stops. If no hole is sensed, paper advance continues until a hole is found.

The levels on the tape may be separated into two groups, Format channels and Advance channels. Levels (or channels) 1 through 6 are Format, and levels 7 and 8 are Advance channels.

If either Advance channel 7 or 8 is selected, paper motion immediately starts and continues until a hole is sensed in the selected channel. Sensing the hole stops paper motion and clears the channel selection. The channel function code must be re-issued to cause another paper movement.

At the end of each print operation, a paper advance is automatically initiated. If none of the 6 Format channels have been previously selected, the paper will automatically advance one line. If a Format channel selection has been made, paper will advance until stopped by a hole sensed in the selected channel. (If more than one Format channel is selected at one time, the first hole sensed stops paper motion.) The Format channel remains selected until a Clear Format function code is received.

The automatic advance may be prevented by sending a Suppress Line Advance on Next Print function code. This will prevent advancing paper on the next print operation, and will then clear. The suppress code must be sent before each Print function for which no line advance is desired.



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE PRINTER CONTROLLER CLOCK		PRODUCT 1612	
	SIZE C		DRAWING NO. 60125000	
	SHEET 70		REV 7	

S.O. 60022 6000 SERIES DATA CHANNEL CONVERTER (170 CARD PUNCH)

CONTENTS

Page	Title
ii	170 Card Punch Controller
1	Function Circuits
2	Punch Characteristics
3	Data Control
5	Data Flow
7	Clock

170 CARD PUNCH CONTROLLER

The CONTROL DATA 6600 Computer System operates the 170 Card Punch Controller via a peripheral controller which simulates a 160 computer I/O interface. In this application, the 170 is connected to an IBM 544 punch.

BASIC PRINCIPLES OF OPERATION

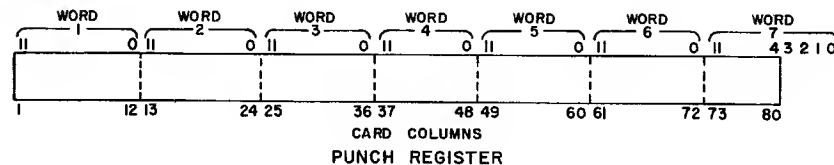
Peripheral and Control Processors communicate with peripheral controllers via a data channel and co-axial signal lines. The controller accepts data and control bits from the data channel register, and one minor cycle later relays these bits to the next controller on that channel. It must also accept data and control bits from that controller and one minor cycle later relay these back to the data channel register.

SELECT CODES

3000	DESELECT	Deselects the punch controller to prevent its responding to codes for other controllers on the same channel. This code should be used at the end of a punch program.
3040	STATUS	Selects the punch controller for an input operation, and the 170 for a status request. The peripheral processor then executes an input instruction to obtain the status reply.
	REPLIES	0000 Ready 2000 Not Ready 0200 Manual Switch in 1604 Position
3002	PUNCH	Selects the punch controller for an output, and the 170 for a punch operation. The 170 immediately starts a card cycle in the 544 punch. The 170 punch selection is cleared at the end of the card cycle, and must be reselected to punch another card.

STATUS. The controller translates a 3040 code, and sends this code, with a Function Ready command, to the 170. The 170 translates the 3040 code and sets the Status flip flop. Status, with Not Punch Select, Punch Ready, and an Input Request from the controller sends the status response and an Input Ready to the controller.

PUNCH SELECT. Translating the 3002 code sets the Punch Select flip-flop in the 170. This sends a clutch enable to the punch, (starting a card cycle) and enables the output gating control. The first output word is gated into positions 1 through 12 of the punch register, with bit 0 to position 12 and bit 11 to position 1. Positions of the punch register correspond to columns on the punch. Output Ready of the first word causes the 170 to send an Output Resume to the controller and advance the output gate to word two. Output word 7 locks the gating control so that no more resumes may be returned to the controller. This condition remains until a row pulse from the punch clears the lockout and resets gating control to word 1. After row 12, the punch sends a punch resume, which clears the punch selection in the 170, thereby dropping the clutch enable. The punch select flip-flop must be set again to reclutch the 544 and punch another card.



PUNCH CHARACTERISTICS

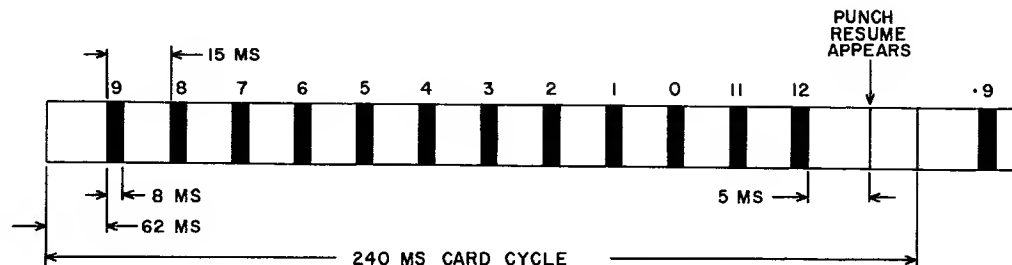
The 544 punches row by row at a maximum rate of 250 cards per minute rate. Cards are placed in the feed hopper face down, "nine" edge first. The Start switch should be pressed to position a card at the punch station before starting a program.

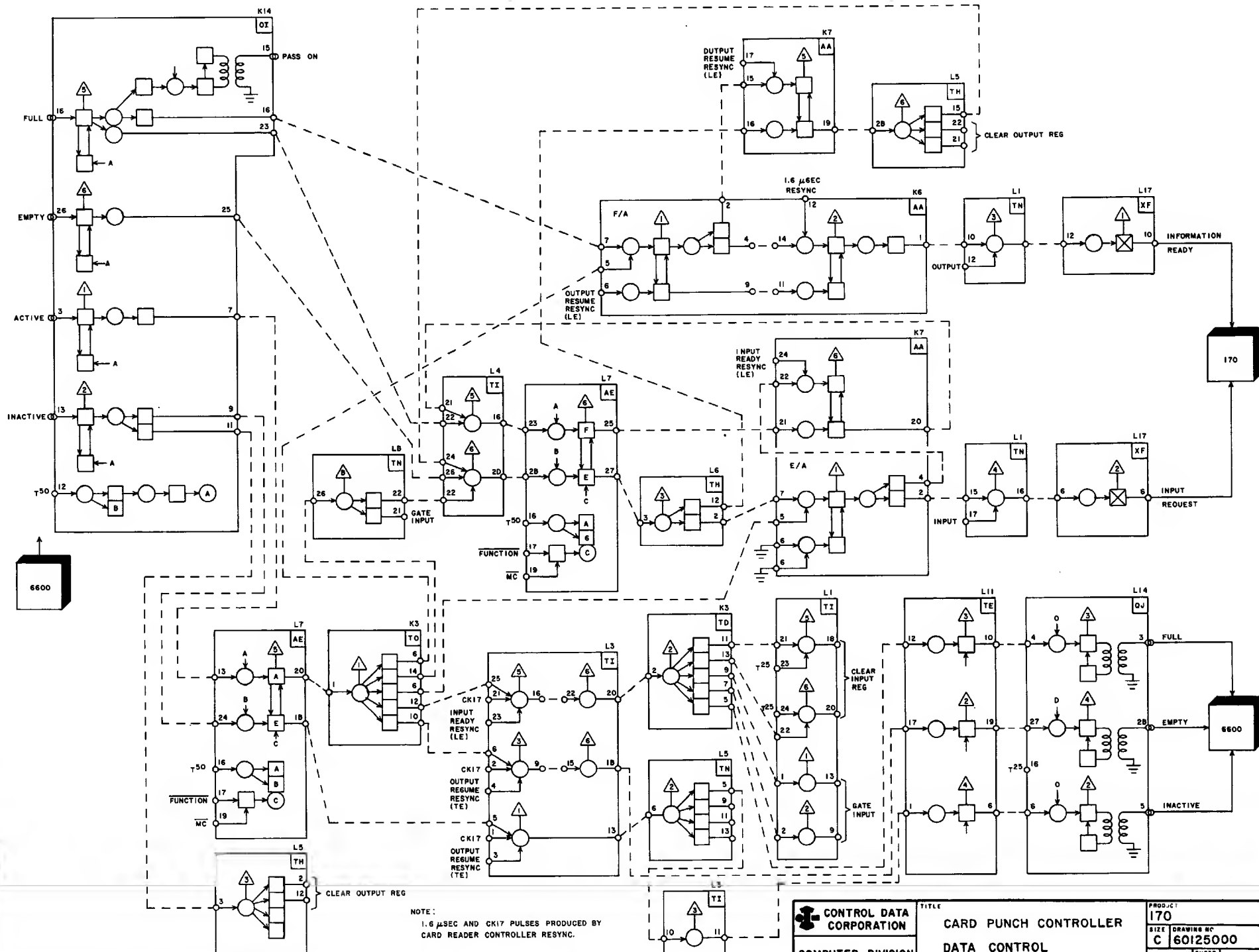
A plugboard is clamped in the front of the 544 cabinet. This may be wired to operate the 544 with the 170 and controller, or to operate the 544 off-line as a gang punch. For details, refer to the IBM 544 manual.

OPERATION. A peripheral and control processor determines the Ready condition by Status Request, selects the 170 for a punch operation, and outputs the data to be punched on one card. An 84-word block is normally established to allow punching one card, and the data sent out on a row-by-row basis.

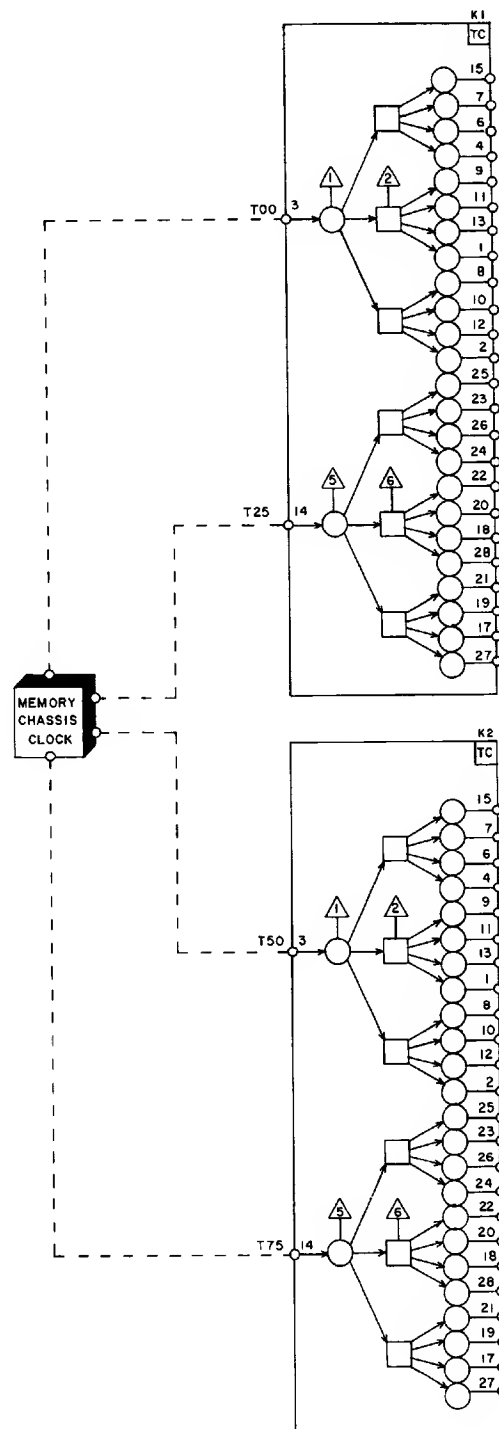
Selecting the 170 for a punch operation sends a Clutch Enable to the 544, starting a card cycle. Near the end of the card cycle, the 544 sends a Punch Resume to the 170. The Punch Resume clears the punch selection in the 170, and enables a Ready status response. The 170 must again be selected to punch another card. For continuous operation, the punch select should be sent as soon as possible after the Ready condition arises.

TIMING. Each card requires 240 milliseconds to pass through the punch station. During each card cycle, the peripheral and control processor must send a select code as well as the data to be punched. The timing chart shows the correct spacing of data outputs, and time for the reselect for one card cycle. All time between row pulses is available for programming.







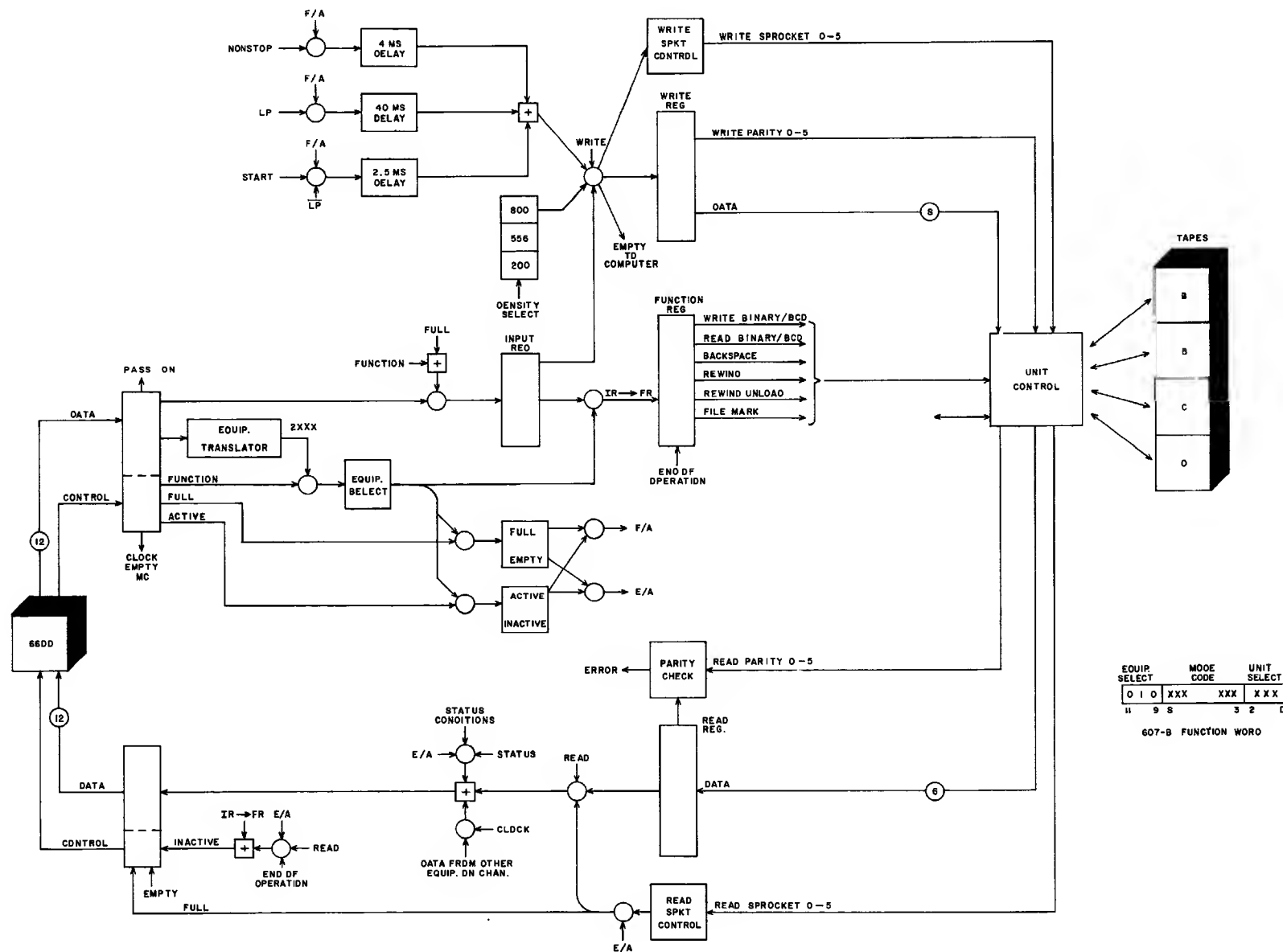


CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CARD PUNCH CONTROLLER CLOCK	PRODUCT 170	
		SIZE C	DRAWING NO. 60125000
		SHEET 74	REV 7

S.O. 60028 6000 SERIES 1 X 4 607 TAPE TRANSPORT CONTROLLER

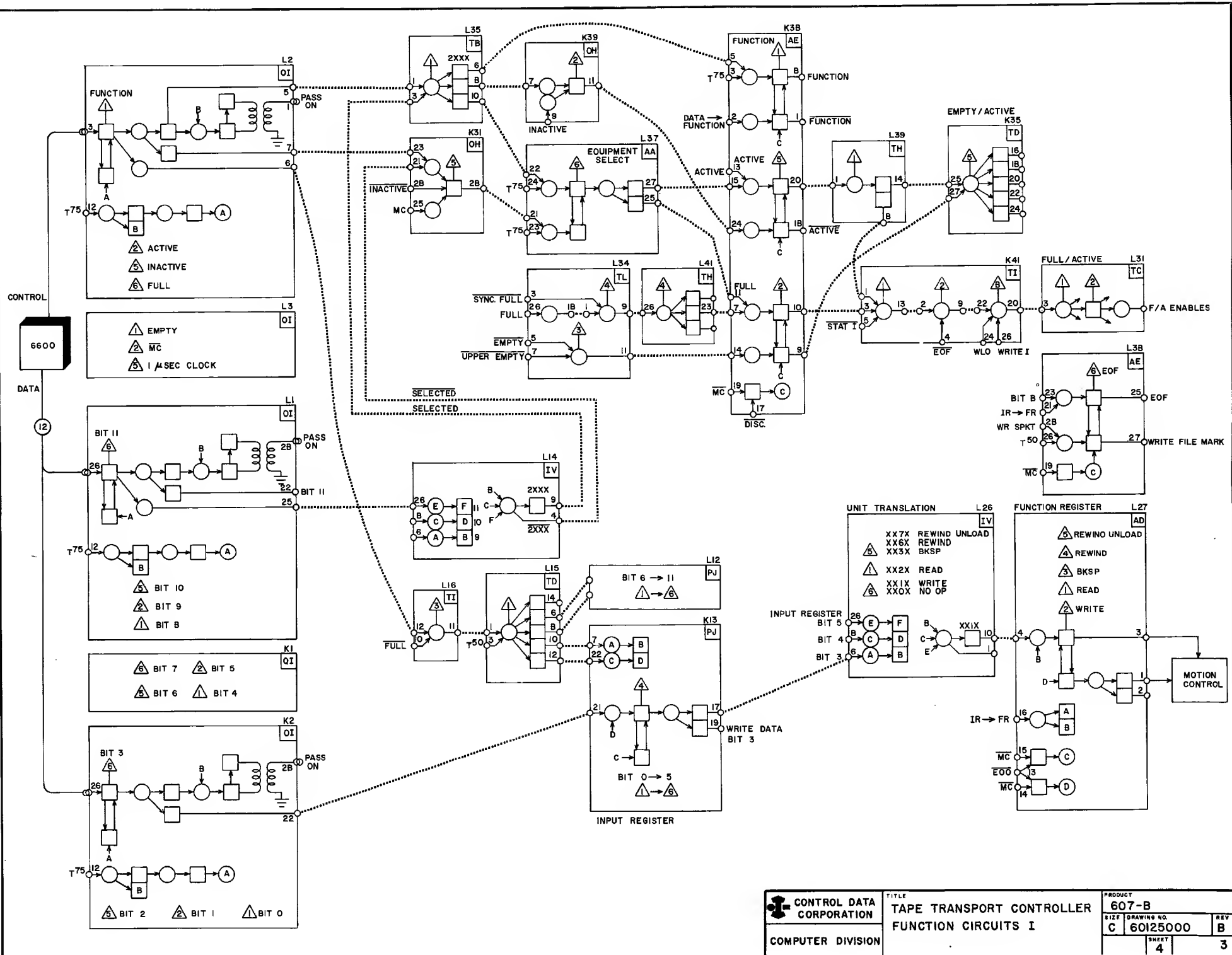
CONTENTS

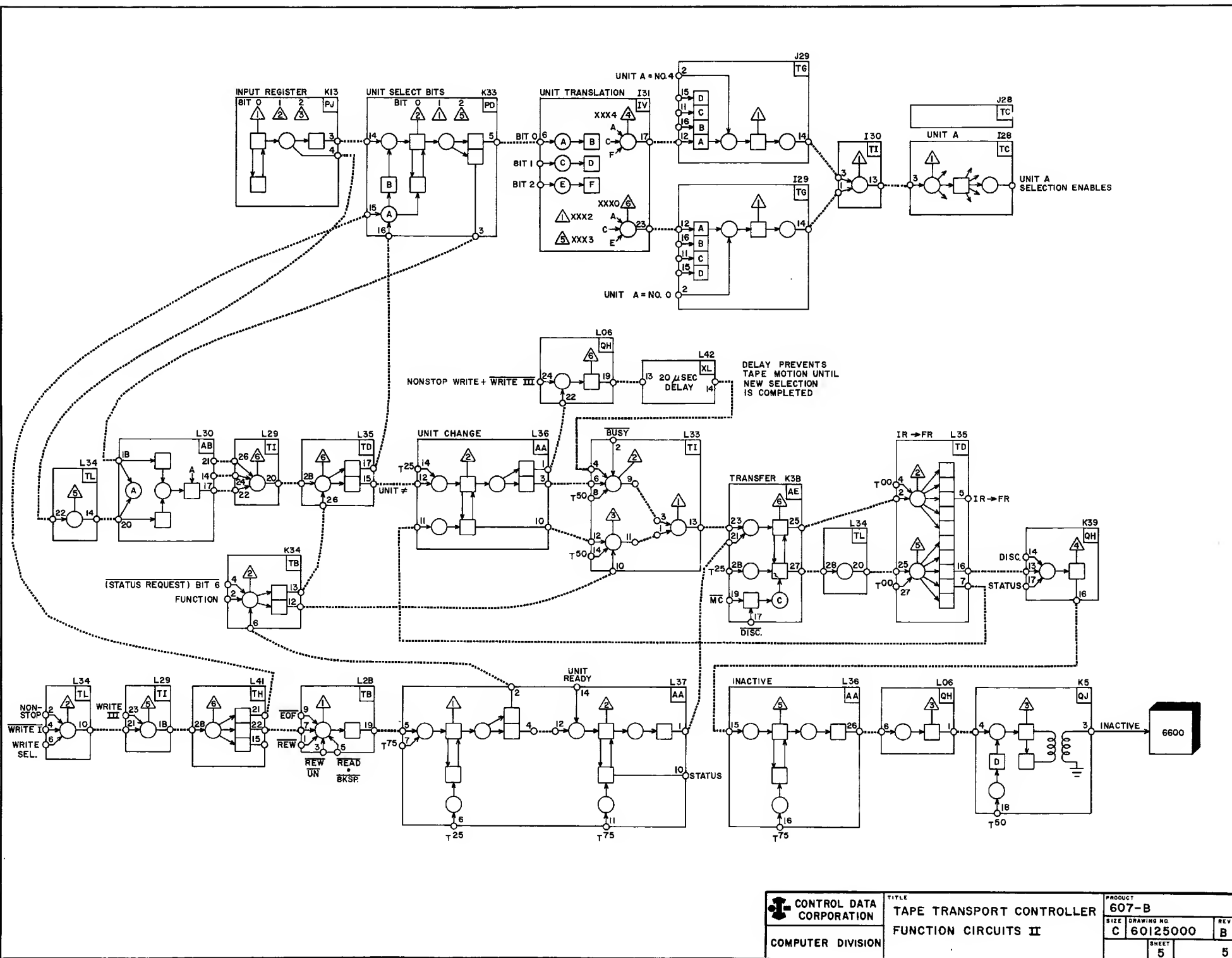
Page	Title
1	Block Diagram
3	Function Circuits I
5	Function Circuits II
7	Unit Control
9	Motion Control
11	Write Osc.
13	Write Data Flow
15	Write Sprocket Control
17	Read Data Flow, Sprocket Control
19	Read Parity Check, End of Record
21	Status Circuits
23	Non-Stop, End of Operation, Busy/Ready
25	Clock

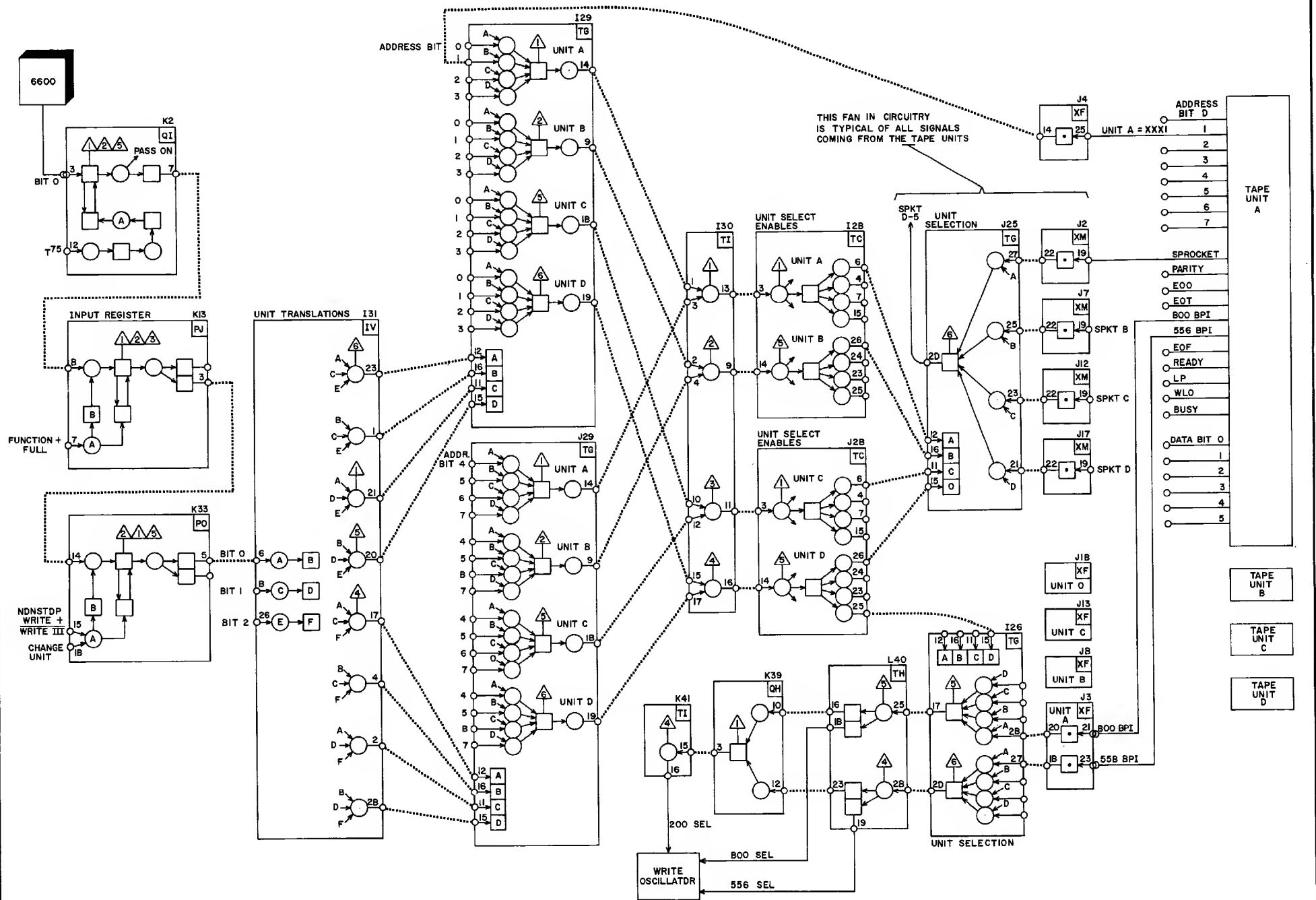


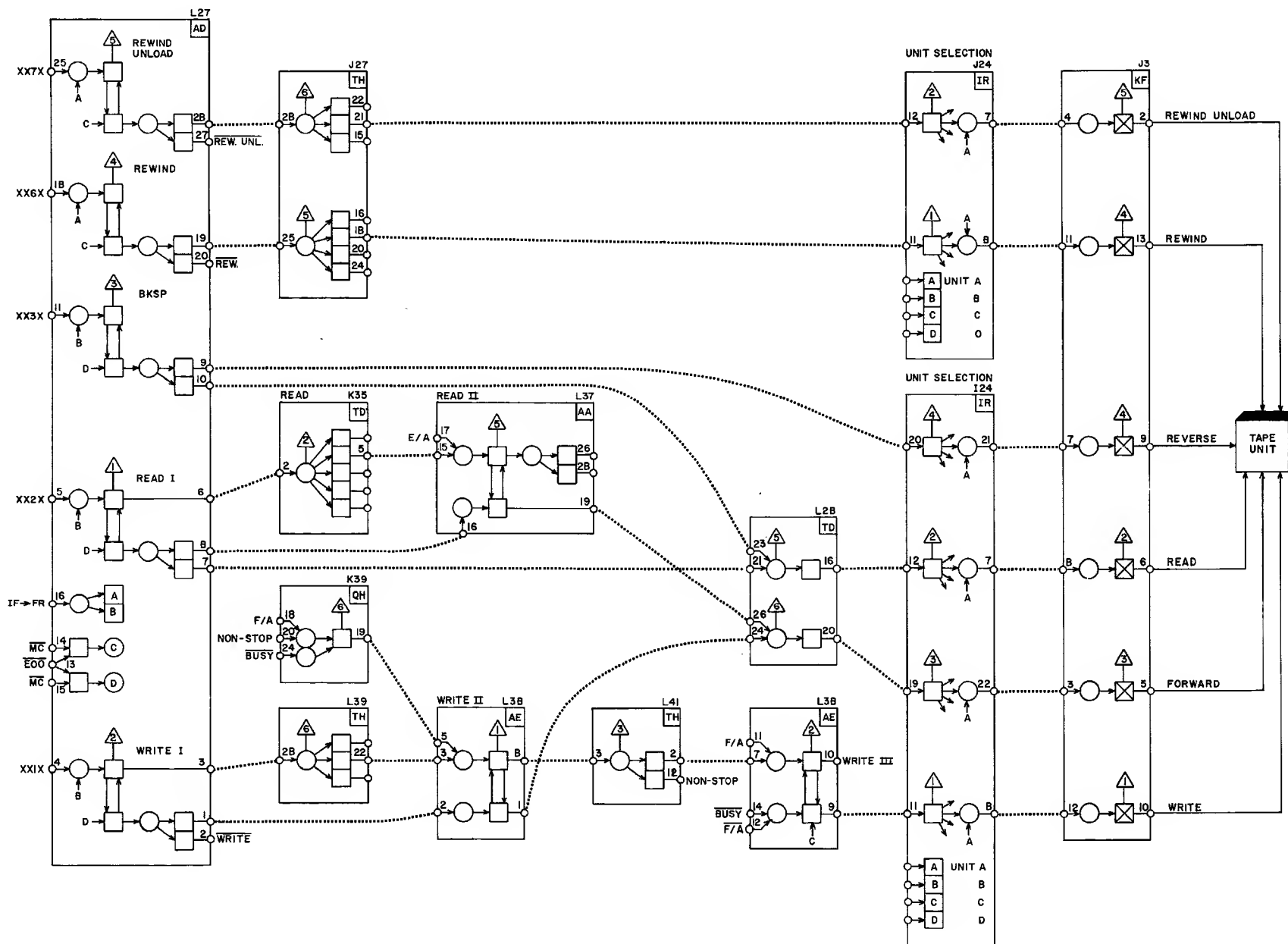
EQUIP. SELECT	MODE CODE	UNIT SELECT
0 1 0	XXX	XXX
11	9 8	3 2 0

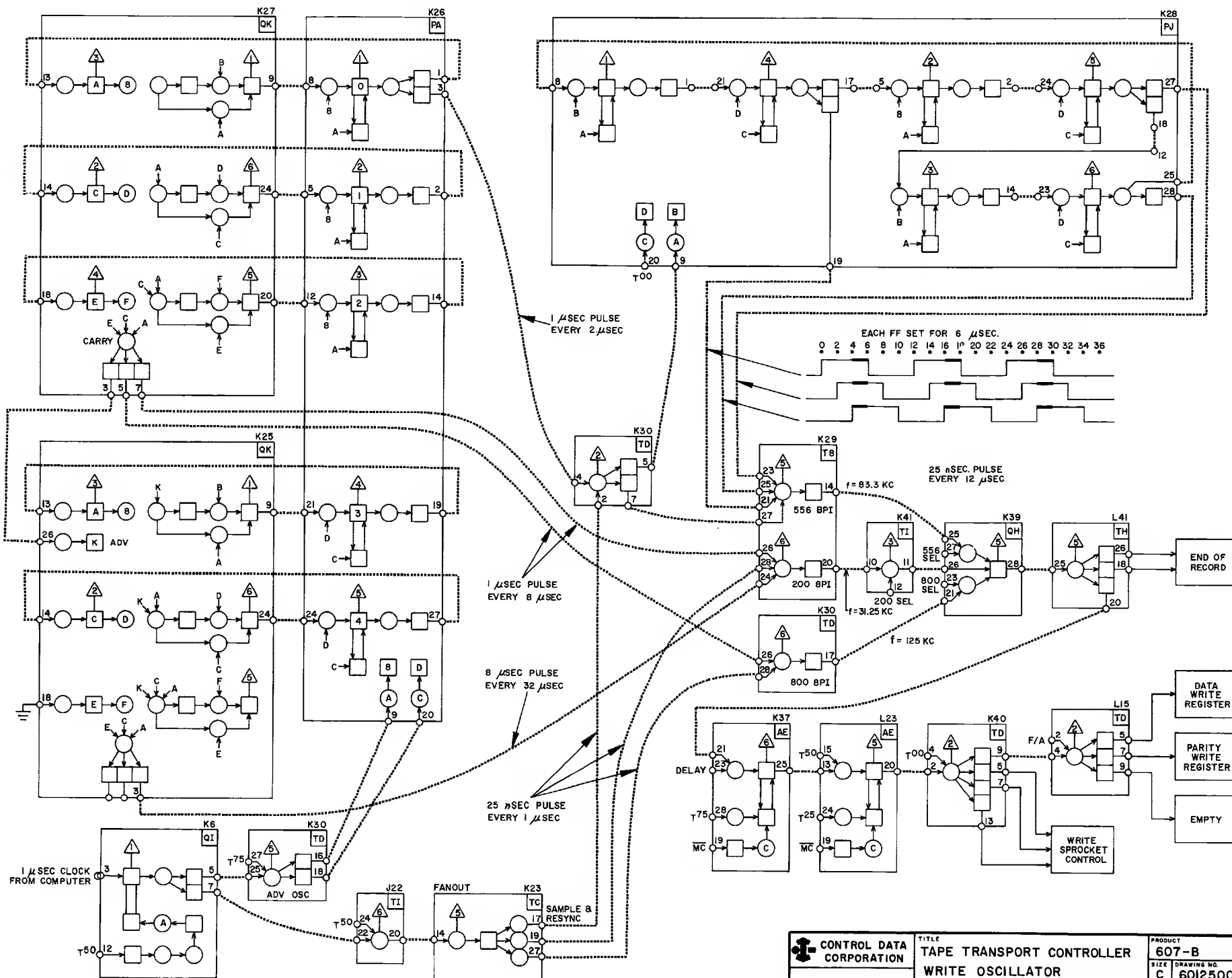
607-B FUNCTION WORD







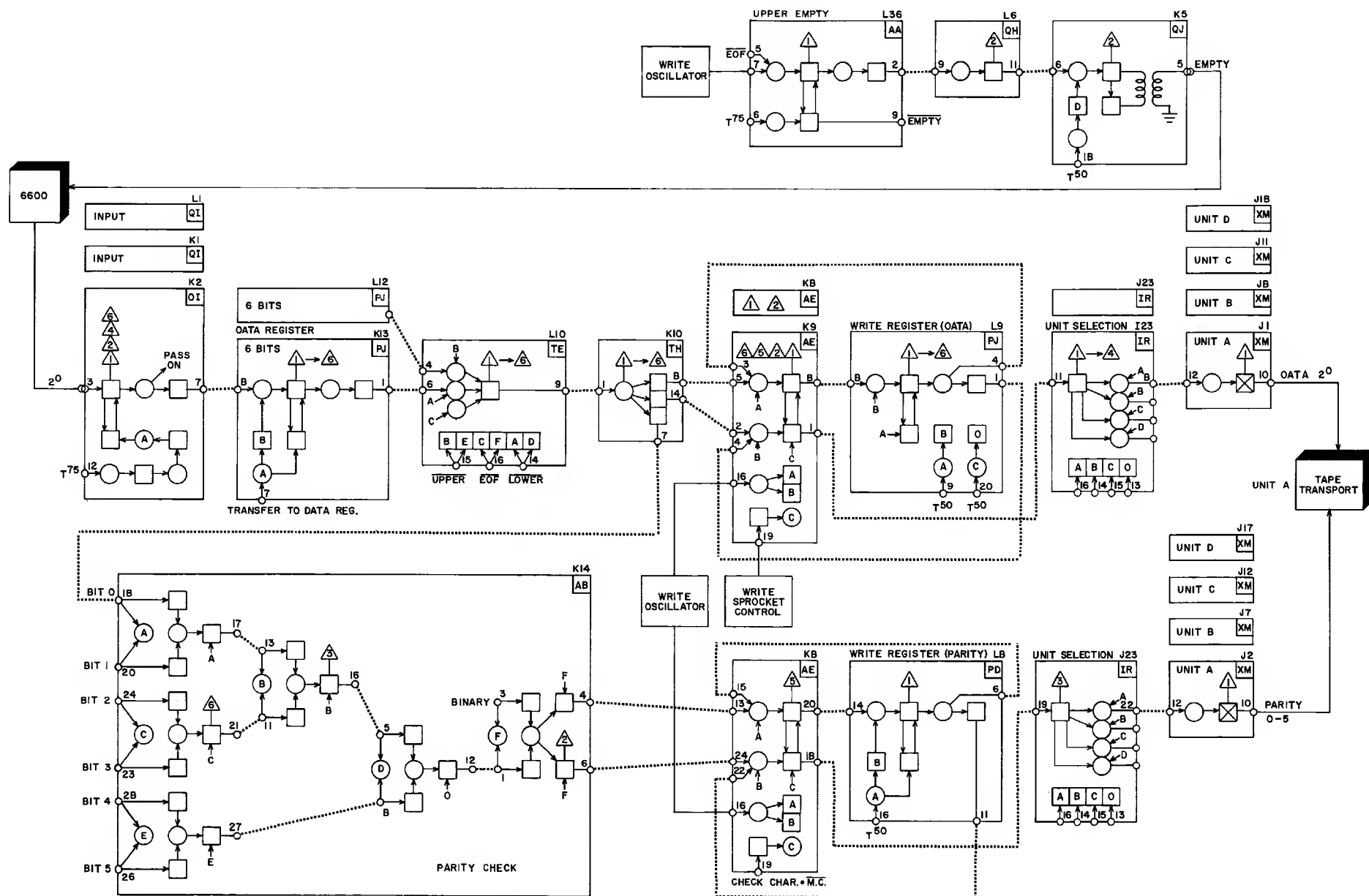


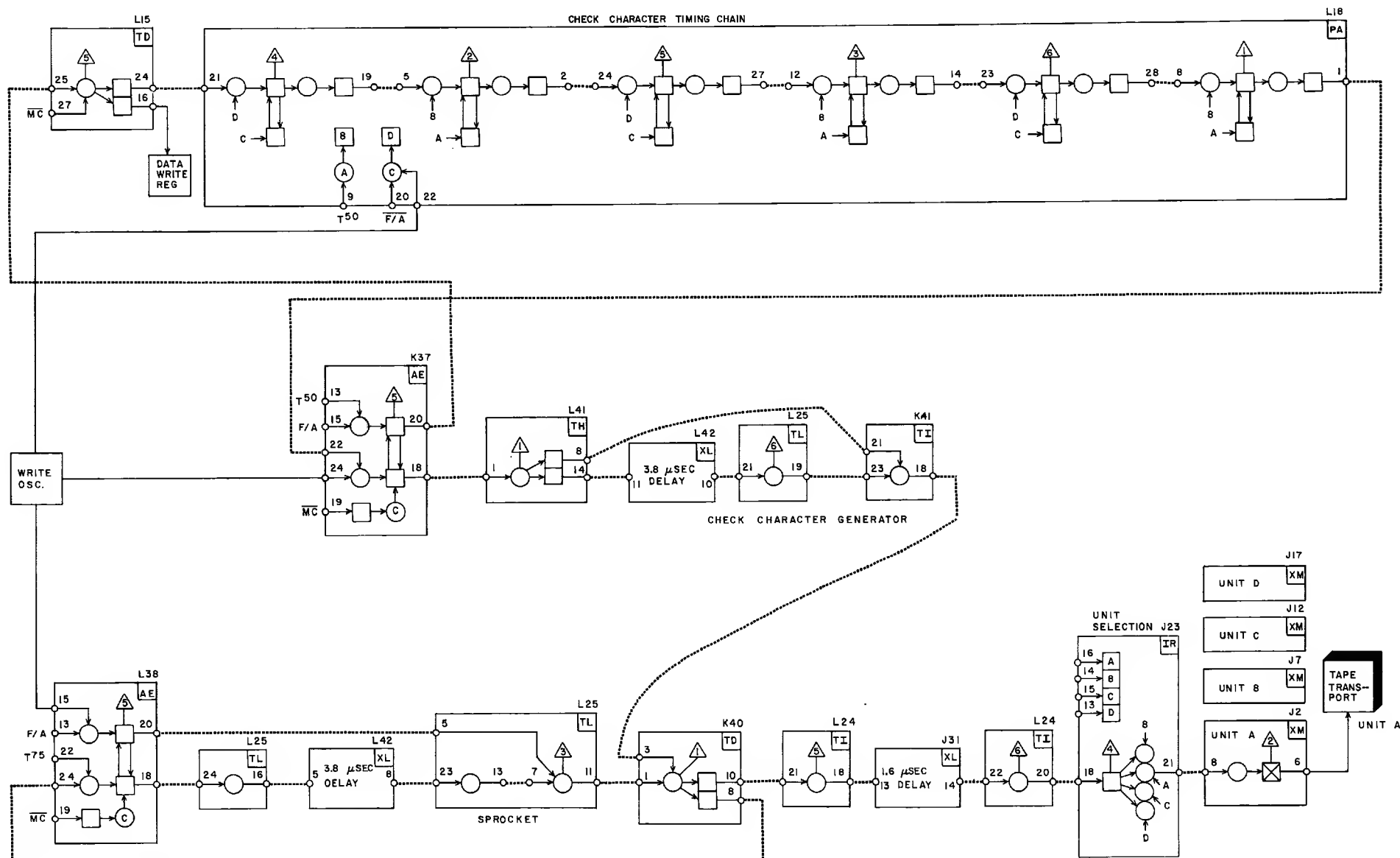


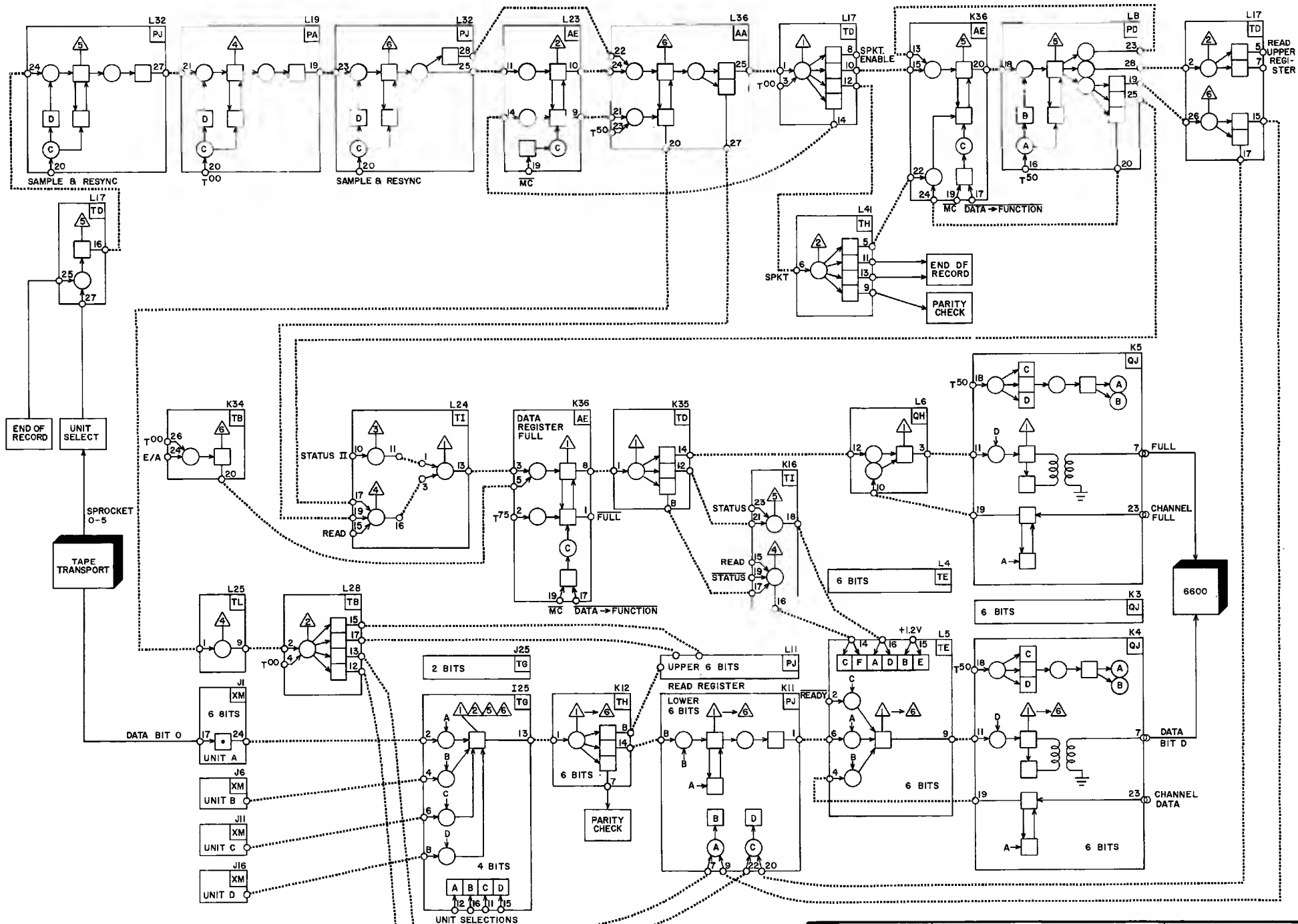
CONTROL DATA
CORPORATION
COMPUTER DIVISION

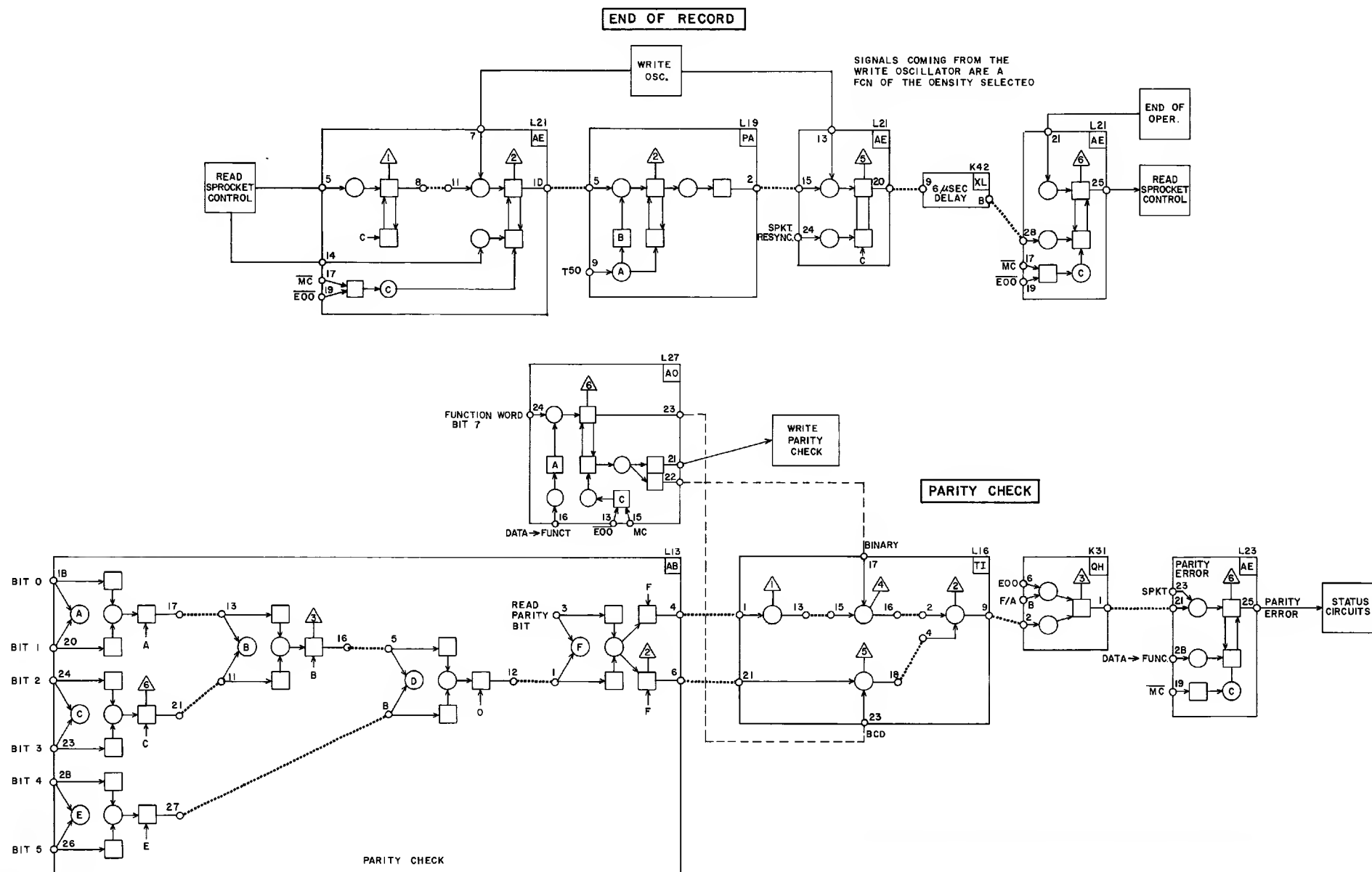
TITLE
TAPE TRANSPORT CONTROLLER
WRITE OSCILLATOR

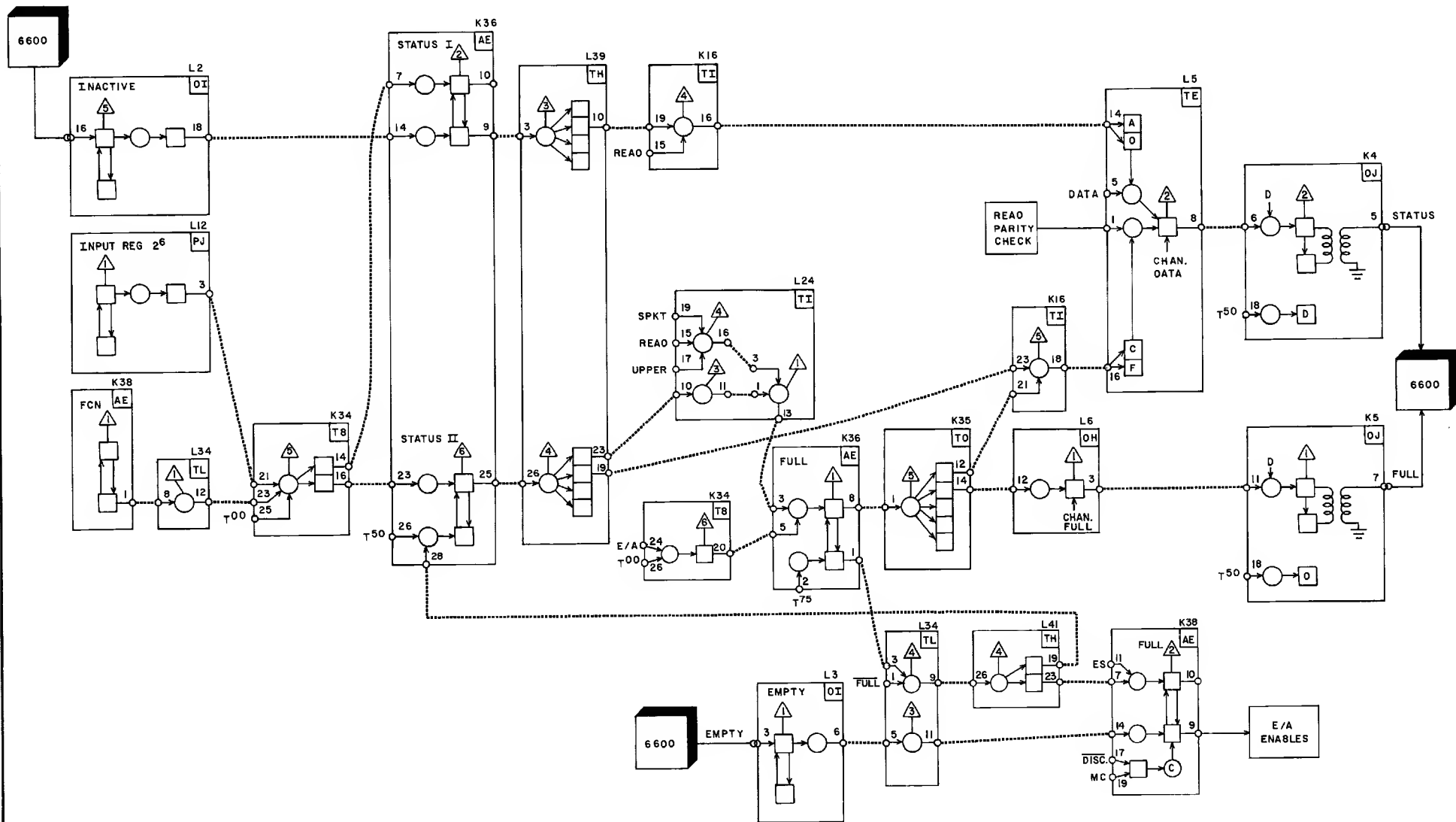
PRODUCT 607-B	
SIZE C	DRAWING NO. 60125000
SHEET 8	REV 8





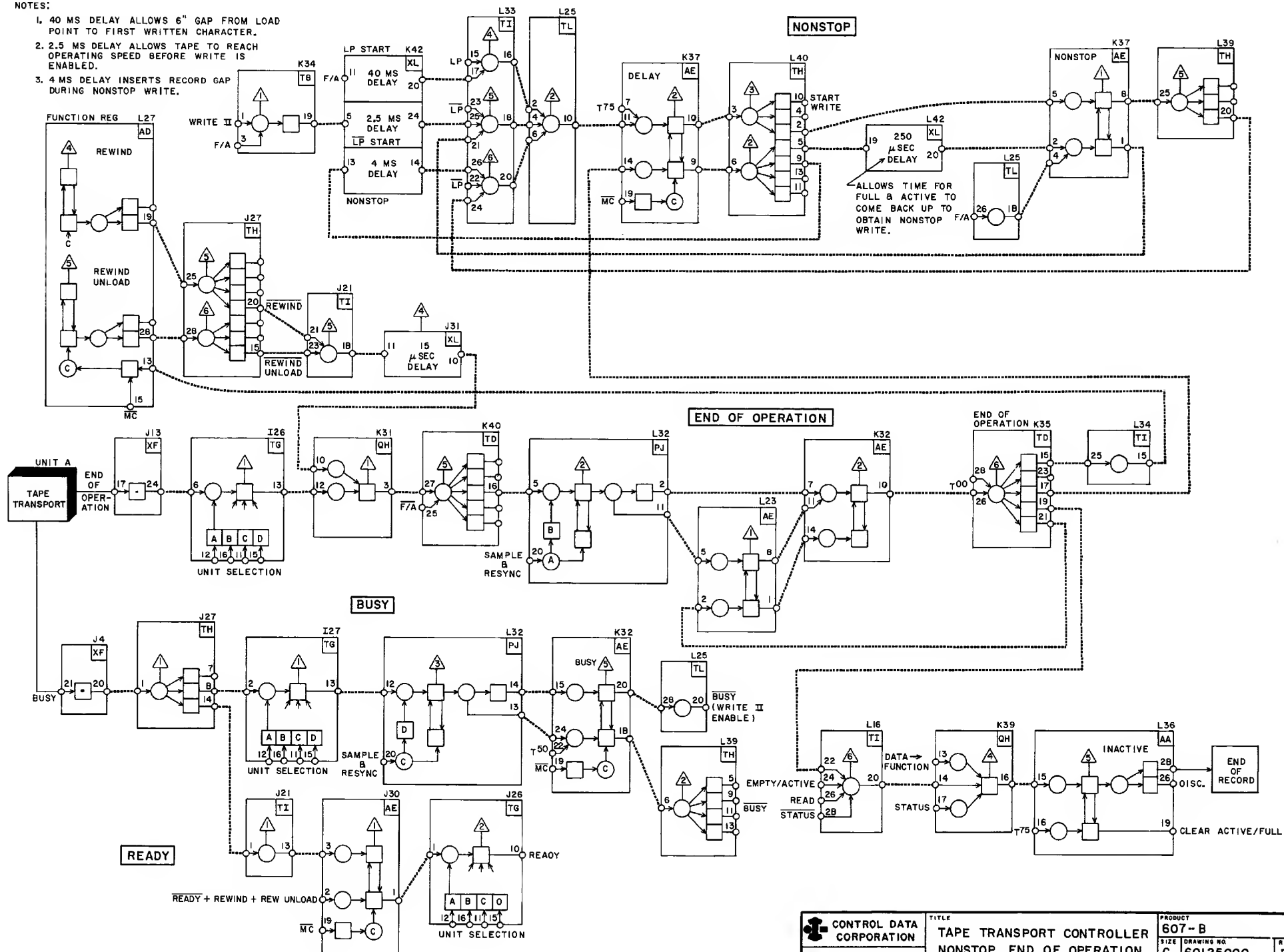


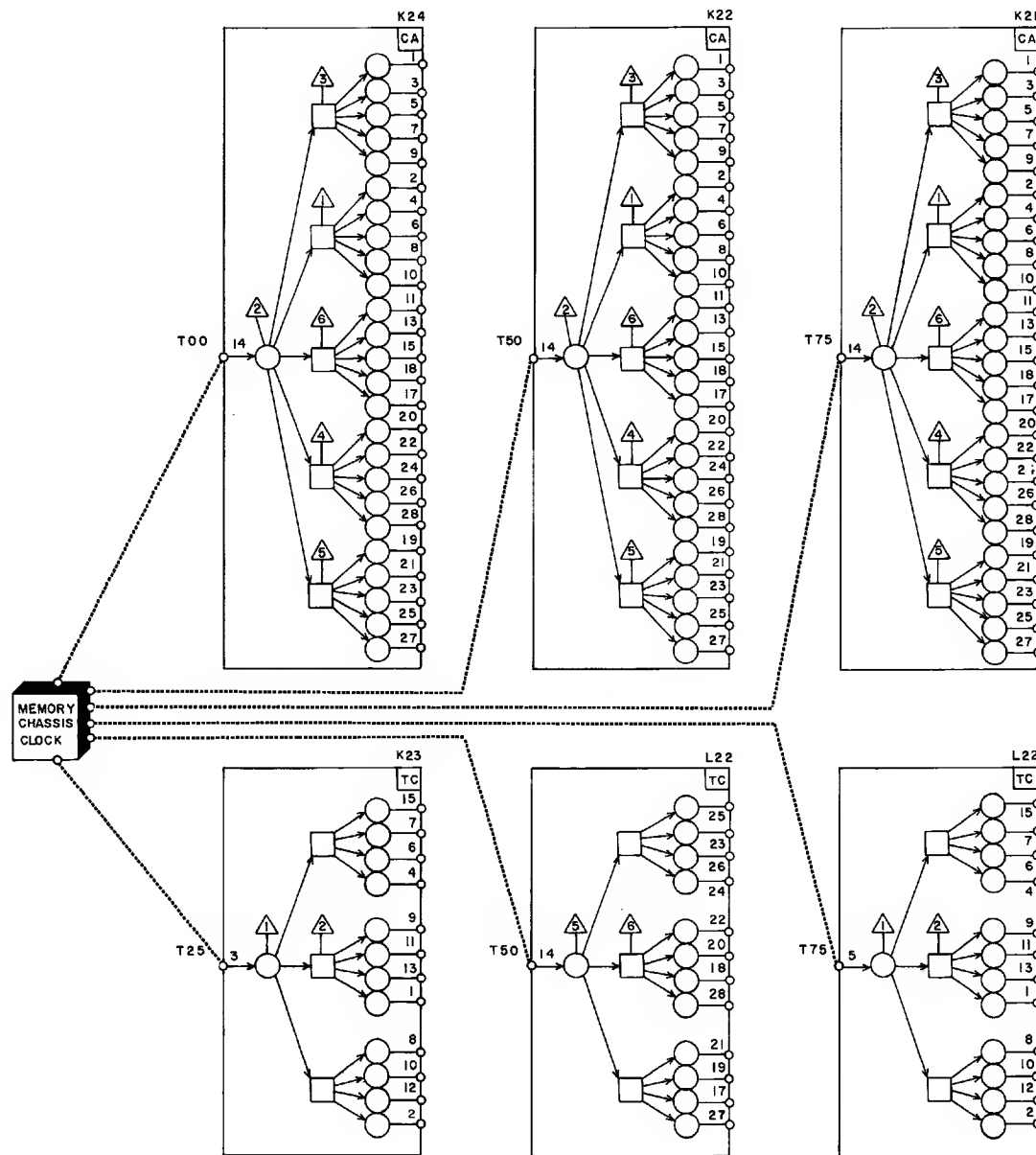




NOTES:

1. 40 MS DELAY ALLOWS 6" GAP FROM LOAD POINT TO FIRST WRITTEN CHARACTER.
2. 2.5 MS DELAY ALLOWS TAPE TO REACH OPERATING SPEED BEFORE WRITE IS ENABLED.
3. 4 MS DELAY INSERTS RECORD GAP DURING NONSTOP WRITE.



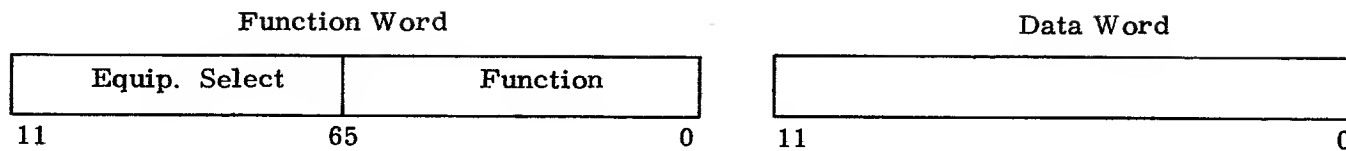


S.O. 60029 6000 SERIES 405 CARD READER CONTROLLER

CONTENTS

Page	Title
ii	405 Card Reader
1	Function Circuits
3	Data Circuits
5	Clock

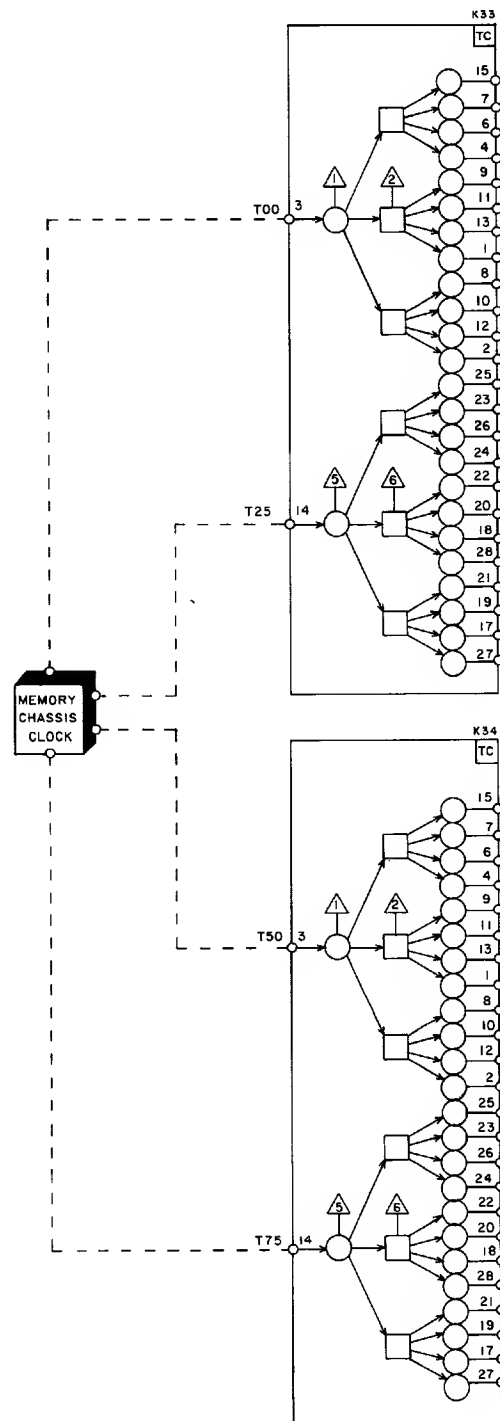
405 CARD READER



0700 De-select
0701 Gate Card to Secondary Bin
0702 Read Non-Stop
0704 Status Request

Reply: 0000 = Ready
0001 = Not Ready
0002 = End of File
0004 = Compare Error

To read one card, execute successive 0702 and 0704 functions.



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CARD READER CONTROLLER CLOCK	PRODUCT 405-B	
		SIZE C	DRAWING NO. 60125000
		SHEET 66	REV 5

COMMENT SHEET
6600 PERIPHERAL CONTROLLERS
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Pub. No. 60125000

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